



Technical Instrument Report ACS 2008-03

ACS-R SMOV Optimization Plan-I Rationale and Strategy

Edward S. Cheng
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ABSTRACT

The document enclosed provides the optimization plan for the Hubble Space Telescope (HST) Advanced Camera for Surveys Replacement (ACS-R) flight hardware. It specifies the rationale for and types of activities required during Servicing Mission Orbital Verification (SMOV) to optimize the on-orbit performance of the hardware. The new flight hardware uses internal interfaces of the instrument that were not described or characterized in detail during the original build of the ACS. This optimization is planned in order to mitigate the risk of the ground (test) hardware not emulating these flight instrument interfaces well enough.

The intent is that the descriptions provided in this document will be further elaborated in detailed SMOV plans, which will then be implemented as a part of the normal HST SMOV flow. The implementation and data analysis will be presented in a companion TIR: ACS 2008-04 "ACS-R SMOV OPTIMIZATION PLAN-II: Implementation and Data Analysis plan."

TECHNICAL MEMORANDUM			
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AUTHOR:	EDWARD S. CHENG		
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2008-MAR-13	INITIAL	ORIGINAL DRAFT VERSION FOR INTERNAL COMMENT.	
2008-APR-27	0.1	REVISED DRAFT FOR COMMENT.	
2008-MAY-18	0.2	REVISION AFTER 2008-MAY-01 DISCUSSIONS. ADD SCIENCE DATA CONTROL REGISTER ADJUSTMENTS. ADD SEQUENCING OF TESTS FOR THE ITERATIONS AFTER REALIZING THAT THEY CAN STEP ON EACH OTHER.	
2008-JUN-21	0.3	REVISION AFTER 2008-MAY-27 DISCUSSIONS. ADD GENERAL DESCRIPTION AND DIAGRAM OF OPTIMIZATION EFFECTS. ADD SPECIFIC RECOMMENDATIONS FROM AW ON OPTIMIZATION SEQUENCE. ADD DESCRIPTION OF ADDITIONAL OPTIMIZATION PARAMETERS.	
2008-JUN-22	0.4	INSERT AW AND ED CHEUNG COMMENTS.	
2008-JUL-04	0.5	UNDERScore NEED FOR Crosstalk MEASUREMENTS IN THE PERFORMANCE ASSESSMENTS, BASED ON THE GROUND-TEST EFFECTS OF MINOR TIMING CHANGES ON Crosstalk. CHANGE INTERFACE DIAGRAM TO REMOVE LVPS2 ELECTRICAL INTERFACE.	
2008-AUG-08	0.6	ADD SPECIFIC VALUES FOR ALL TABLES (EXCEPT SCIENCE DATA CONTROL REGISTER TESTS, WHICH ARE STILL RELATIVE TO POST-TV DERIVED VALUES). ADJUST OSCILLOSCOPE MODE INTERNAL SIGNALS TEST CASES. SPECIFY MORE MACRO NAMES FOR CLARITY. ADJUST SCHEDULE TO EXTEND UNREALISTIC 1-DAY THINKING TIME FOR ITERATION 2. OTHER SMALL CLARIFICATIONS FROM THE REVIEW ON 2008-JUL-25. ADD A RELEASE NOTES SECTION TO STATE POTENTIALLY TIME-DEPENDENT ASSUMPTIONS. OCTOBER 8 LAUNCH DATE REQUIRES ADJUSTMENT OF THE SMS START DAY FOR ACS-R. EXTENDED THE CAMPAIGN TO ACCOMMODATE SMS BOUNDARIES. FINAL PRE-RELEASE VERSION.	
2008-AUG-09	0.7	SYNCHRONIZE TEXT WITH MARKUS' CONFIGURATION TABLE FOR SECTION 6.1.4. RESTRUCTURED THE TABLE IN THAT SECTION FOR CLARITY.	
2008-AUG-18	1.0	RELEASED VERSION.	
APPROVALS			
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-	NONE REQUIRED		

1 SCOPE

This TM provides the optimization plan for the Hubble Space Telescope (HST) Advanced Camera for Surveys Replacement (ACS-R) flight hardware. It specifies the rationale for and types of activities required during Servicing Mission Orbital Verification (SMOV) to optimize the on-orbit performance of the hardware. The new flight hardware uses internal interfaces of the instrument that were not described or characterized in detail during the original build of the ACS. This optimization is planned in order to mitigate the risk of the ground (test) hardware not emulating these flight instrument interfaces well enough.

The intent is that the descriptions provided in this document will be further elaborated in detailed SMOV plans, which will then be implemented as a part of the normal HST SMOV flow.

2 APPLICABLE DOCUMENTS

Hubble Space Telescope Advanced Camera for Surveys (ACS) Repair End Item Specification, December 2007, STE-83.

ACS Repair PDR Package, June 20/21, 2007.

ACS Repair CDR Package, October 3/4, 2007.

ACS-R Verification Plan, 2008-Jan-10, CcA-2008-01-01.

O-Scope Design Concept: Preliminary Discussion and Review, undated but sent March 6, 2008, Powerpoint, Raphael Ricardo/TIS.

CEB-R Translator FPGA Design Description Document, May 14, 2008, Ed Cheung/J&T

3 ACRONYMS

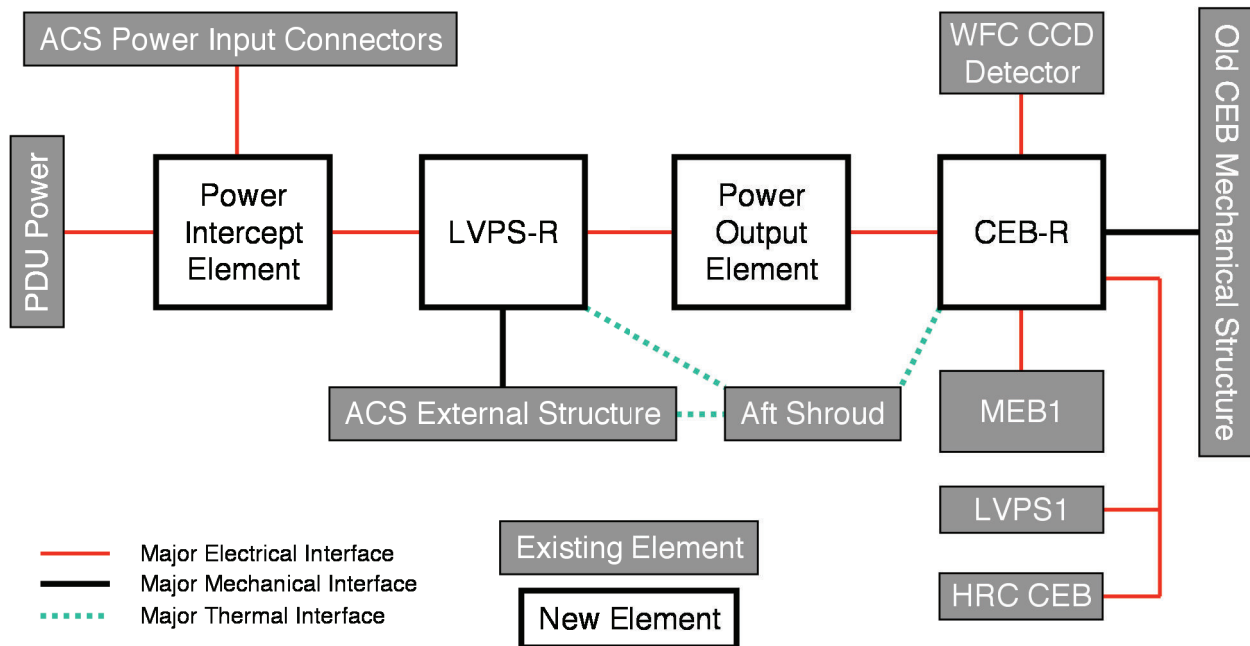
ACS	Advanced Camera for Surveys
ASIC	Application-Specific Integrated Circuit (usually refers to the SIDECAR)
C&S	Clamp-and-Sample
CCD	Charge-Coupled Device
CDR	Critical Design Review
CEB	CCD Electronics Box (the original version for ACS)
CEB-R	CCD Electronics Box Replacement (the version for ACS-R)
CTE	Charge Transfer Efficiency
DCL	Detector Characterization Laboratory (at NASA GSFC)
DSI	Dual-Slope Integrator
EGSE	Electrical Ground Support Equipment
EM	Engineering Model
ESTIF	Extended Software Test and Integration Facility
EVA	Extra-Vehicular Activity
FAC	Flight Assembly Code
FM	Flight Model
FS	Flight Spare
FSW	Flight Software
GSE	Ground Support Equipment
GSFC	Goddard Space Flight Center
HST	Hubble Space Telescope
J&T	Jackson and Tull
LVPS	Low-Voltage Power Supply
LVPS-R	Low-Voltage Power Supply Replacement
MEB	Main Electronics Box
PDR	Preliminary Design Review
PDU	Power Distribution Unit
PIE	Power Intercept Element (LVPS-R input harness)
POE	Power Output Element (LVPS-R output harness)
SDCR	Science Data Control Register
SIDECAR	System for Image Digitization, Enhancement, Control And Retrieval
SITe	Scientific Imaging Technologies, Inc. (no longer in existence)
SM4	Servicing Mission 4
SMS	Science Mission Specification
TBD	To Be Determined
TBR	To Be Resolved
TIS	Teledyne Imaging Sensors
TM	Technical Memorandum
VSTIF	VEST Software Test and Integration Facility
WFC	Wide Field Channel

4 General

The ACS Repair (ACS-R) flight hardware consists of the following major components:

1. The CCD Electronics Box Replacement (CEB-R),
2. The Low Voltage Power Supply Replacement (LVPS-R),
3. The Power Input Element (PIE), and
4. The Power Output Element (POE).

The diagram below summarizes their relationship. This hardware will be verified by ground testing according to the ACS-R Verification Plan.



The ground verification program is designed to ensure, as far as possible, that the ACS-R hardware will perform as expected with the on-orbit hardware and meet performance requirements. Nevertheless, because the ACS-R hardware replaces internal subsystems within the ACS instrument, the level of verification is at best by “similarity” to the on-orbit systems. This poses some inherent risks that need to be mitigated by on-orbit flexibility where possible.

4.1 Installation Risks

During installation, the mechanical system has the highest risk, especially the installation of the CEB-R into the existing CEB chassis after the old boards are removed. This risk is mitigated by appropriate design and tolerance analyses, and by worst-case mechanical alignment testing during the verification program.

4.2 Post-Installation Risks

After installation, the electrical system risks dominate. The ACS-R must first draw power from the PIE. This is readily checked since it is a well-established interface with the spacecraft.

The CEB-R must also communicate with the ACS MEB. This is a less well-defined interface because it is an internal instrument interface. However, the ground test equipment (Ops Benches) have MEB-equivalents in them for verification. These MEB-equivalents are electrical duplicates of the on-orbit MEBs and should present high-fidelity copies of the on-orbit interfaces. There is one in the VSTIF and one in the ESTIF.

Finally, the CEB-R must control and read out the ACS WFC CCDs. This aspect is the most problematic, and has driven many of the design features for on-orbit flexibility.

Ground testing can help ensure that the CEB-R is capable of reading out flight-representative (same manufacturer, same design) CCDs, but the performance of these SITe CCDs is highly variable from device to device. As discussed below, there is also evidence of some variability in the transient response of the external preamp that is attached to the detector housing. Thus, it is very hard to ensure that the ground devices and configurations are the same as those on orbit for all critical parameters. This is especially true since the on-orbit devices have had several years of radiation exposure, which is known to adversely affect CCD performance and electronics performance in general.

Ground testing has revealed some non-ideal transient settling behavior in the preamp that is attached to the flight-like detectors. This subsystem is already on-orbit, and is not modifiable by ACS-R. Since this is an internal interface (CCD to CEB), it was not particularly well-documented nor was it well-tested in isolation. The requirement (and verification) had been on the subsystem that includes the CCD and CEB. Nevertheless, the behavior of these preamps can impact the effectiveness of the video processing circuitry within the CEB-R, and needs to be accommodated by the CEB-R hardware. We can get a good idea of the range of behavior from ground testing, but the CEB-R will need to be adapted on-orbit for the flight preamp behavior.

Ground testing has also revealed a noise dependence on the exact timing of the science data transmission (from the CEB-R to the MEB) relative to the pixel processing timing. The Science Data Control Register described in the "CEB-R Translator FPGA Design Description Document" was invented to allow for optimizing the placement of the noisy data transmission time periods by separating them into two shorter periods and moving them away from critical times in the pixel processing.

To mitigate these risks, the CEB-R has been made to be as flexible as reasonably possible to allow for on-orbit adjustments to optimize its operation with the flight CCDs. The main areas of designed-in adjustment are:

1. CCD bias voltages (9 distinct values). These voltages provide power to various elements inside the CCD, including the output stage.

2. CCD clock rail voltages (12 distinct values). These voltages control the analog charge shifting function within the CCD.
3. CCD readout timing pattern (44 16-bit words for each pattern). These patterns control the waveforms and phasing of the clocks to shift the charges to the CCD output amplifiers, control the CCD output amplifiers, and control the video processing circuitry to interpret the CCD output amplifier output voltages.
4. The Science Data Control Register in the FPGA can be set to control the detailed timing of the science data transmission from the CEB-R to the MEB. This adjustment allows for splitting up the 16-bit transmission (for every pixel) into two parts, each with an arbitrary offset in time relative to when the ASIC completes its data transmission to the FPGA.
5. The SIDECAR ASIC that generates these signals is fully programmable and the Flight Assembly Code (FAC) could be modified on-orbit to accommodate other effects. Obviously, this level of “adjustment” will be avoided if at all possible.

After installation, these adjustment areas will need to be optimized for the on-orbit hardware before we can expect to reach the level of performance achieved in ground testing. This rationale and strategy for this optimization is the topic of this TM. From this, several areas of detailed planning will be needed (with rough indications of the responsible parties).

1. Operations planning (Ops/STScI).
2. Operations implementation (STScI/Ops).
3. Optimization strategy (ACS-R).
4. Observation scheduling (SMS-level) and data return (STScI).
5. Data analysis planning (ACS-R/STScI).
6. Realtime uplink planning (Ops/STScI).

Since the optimization activities will mostly occur during the Servicing Mission Orbital Verification (SMOV) phase after HST re-deployment, they will have a significant impact on the SMOV planning. Some tests may also be requested as a part of the ACS-R Functional Test after installation so that the optimization process can begin before the start of the allocated SMOV optimization time (anticipated to be several days later).

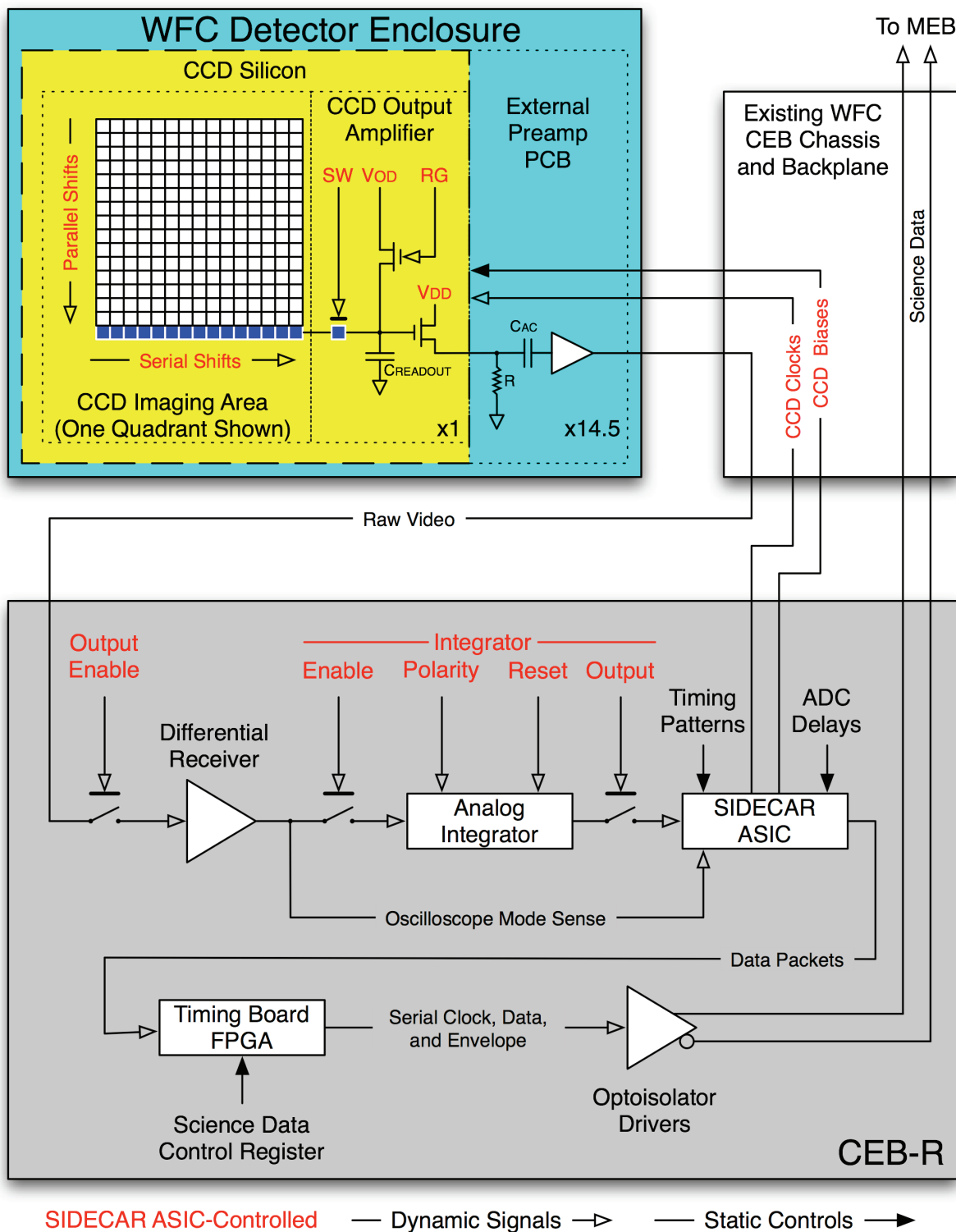
4.3 The Requirements

Here is what we are trying to achieve, stated in requirement form.

The ACS-R, upon installation into HST, shall provide the *capability* of meeting the final performance requirements. Performance optimization shall be completed during SMOV using special (internal) observations. At the end of the on-orbit Optimization Campaign during SMOV for SM4, the ACS-R shall provide a level of performance for the ACS Wide Field Channel (WFC) that is at least as good as the original CEB. The ACS-R shall provide this performance with the same operations concept as the original CEB. In particular, further internal adjustments shall not be required to maintain the desired performance of the CEB-R (but could still be required to compensate for CCD degradation effects, as with the original CEB).

4.4 System Description

The following block diagram provides a top-level description of the system being optimized.



Starting from the upper left, the first element is the on-orbit ACS WFC Detector Enclosure. This element is not being replaced by ACS-R activities. It houses two 2K x

4K SITe CCDs that are mosaiced into a 4K x 4K format. The two CCDs are electrically independent. The diagram shows one quadrant of this detector (half of one of the CCDs). The imaging area collects charge, which is shifted (down) by appropriate “parallel” clocking into the serial shift register, and which is then shifted (right) by “serial” clocking towards the Summing Well (SW). The clocks are controlled by Timing Patterns within the ASIC.

The next processing element is the CCD Output Amplifier. At the start of a readout period for a pixel and before the charge arrives at the amplifier for that pixel, the amplifier is reset by briefly activating Reset Gate (RG). When reset, the capacitor at the input to this voltage follower (C_{READOUT}) is set to a certain voltage determined by RG and the bias V_{OD} . The output of the amplifier then reads the “reference” phase of the video signal for a particular pixel. This phase is held for a little less than half of the 22 μs pixel period.

The SW is then activated to transfer the charge for a pixel onto the input capacitor. This capacitor converts the charge into a voltage, and changes the voltage at the capacitor (from that during the reference phase) by an amount proportional to the charge deposited. This voltage is buffered by the CCD Output Amplifier and sent to an External Preamp that is located right outside the Detector Enclosure on a printed circuit board. The period after the SW activation is the “signal” phase of the video signal for a particular pixel. The amount of light seen by a pixel is, to first order, the difference between the reference and signal phases of the video signal.

After amplification, the video output signal is conveyed by existing wiring harnesses within ACS to the WFC CEB chassis connector and backplane. This chassis and backplane is also not replaced by ACS-R activities. The new CEB-R is inserted into this chassis and mated with the backplane after removal of the old printed circuit boards in the old ACS CEB.

The bottom part of the diagram with the grey background shows some blocks within the new CEB-R. An Output Enable switch controls whether the CEB-R internal differential amplifier is sensing the input line. This switch protects against large voltages that may appear on the video when the CCD Output Amplifier is being reset. These voltages are not damaging to the CEB-R, but affect performance because they could saturate the CEB-R electronics, causing long and unnecessary recovery times. Appropriately controlling the timing of this switch makes sure that the internal electronics are not overdriven, so that dynamic performance and saturation recovery is limited by the External Preamp.

The output of this differential amplifier is the signal that is sensed by the Oscilloscope Mode of the CEB-R. There is one Oscilloscope Mode signal for each of the four output amplifiers of the CCD. These signals are sent directly to the ASIC for digitization.

For clarity, only the Dual-Slope Integrator (DSI) video processing scheme is now described. A brief discussion at the end summarizes the Clamp-and-Sample scheme. These two schemes are *functionally* equivalent, in that they both provide digitized science data output based on the light detected by the CCDs. They will differ in *performance*. It is believed that the Dual-Slope Integrator will have better noise performance based on design as well as ground testing. Because the old CEB uses a

Clamp-and-Sample scheme, this was also included in the new CEB-R in the event that the Dual-Slope Integrator encounters an unexpected problem when working with the on-orbit instrument. These two video processing schemes are selected by changing a bit in an ASIC register.

The integrator is designed to subtract the time integral of the reference phase from the time integral of the signal phase of the video signal. The Integrate Enable control determines whether the integrator is actively integrating or is in a “hold” state where its output voltage is not affected by the input. The Integrate Polarity control determines whether the integrator is integrating the signal with a positive or negative polarity. Finally, the Integrator Reset control resets the integrator output voltage to a preset value. At the start of a pixel, and when the CCD Output Amplifier is being reset, the integrator is also disabled and reset (and the Output Enable disables the video). After some delay time (nominally 4 μs) to allow for External Preamp recovery and serial clock feedthrough, the integrator is enabled to integrate the reference phase down (nominally 7 μs). The SW is then activated to transfer the charge to the CCD Output Amplifier. During this time (nominally 3 μs), the integrator is disabled. The signal phase then begins, and the integrator is set to integrate up (for nominally 7 μs). The integrator is then disabled to hold the signal for the ASIC, and the integrator output is connected to the ASIC input (nominally 1 μs).

At the end of each pixel period, the ASIC looks at the integrator output and converts the voltage into a digital value. These numbers are then transmitted to the Timing Board FPGA, which then transmits these numbers to the ACS MEB. The detailed timing of these data transmissions is controlled by ASIC ADC delays as well as the FPGA Science Data Control Register.

For the Clamp-and-Sample the only difference is in the block that is labeled “Analog Integrator”. Instead of integrating the signal, the bandwidth of the signal is reduced using a low-pass filter (to reduce the effective noise bandwidth). This filtered video voltage is clamped to a reference voltage (say 0 volts) on a capacitor during the reference phase. This clamp is then released, and the transition in the video voltage to the signal phase changes the capacitor voltage by the amount we are trying to measure. At the end of a pixel time, the ASIC converts this voltage into a digital value.

4.5 Release Notes

As of the release date of this document, the FM1 Oscilloscope Mode function is not working perfectly. On the primary ASIC side, channels A and B work fine when looking at CCD outputs A and B, but channels C and D exhibit a strange noise. This is believed to be caused by signal routing issues. On the redundant side, channels A and B are not reliable, but channels C and D are fine. The Oscilloscope Mode tests in Section 6.1.4 can be adjusted to account for this as much as possible.

The integration time of the DSI was previously 8 μs for the reference phase and 8 μs for the signal phase, with a 1 μs disabled state for the SW clock. It appears that the A->B and C->D channel crosstalk is very bad (~1 part in 1000) for this timing, but can be dramatically improved by increasing the SW disable time to 3 μs . This is now the

default, and provides 7 μs integration for the reference and signal phases. The impact on noise turns out to be negligible. This late change may not be propagated through all the documentation.

Testing still has to be performed to determine the nominal settings for the Science Data Control Register in Section 5.6. These tests will be done in the DCL with EM1 when it is retrofitted with the flight-like “brown” ASPC/Bias board.

5 Main Concerns and Quantification/Optimization Strategy

The main concerns for optimizing the on-orbit performance of the CEB-R when operated with the flight CCDs fall into the following general categories. The order below is somewhat arbitrary, and the general concept is to go from things that have “pixel scale” effects to those that have more global effects.

In the sections below, the main concern is described, as well as sample data that could be acquired to address the concern. These data sets are intended to be illustrative examples, and may not represent the most efficient manner to collect the information. They can (and should) be modified appropriately during implementation planning to be as efficient as possible.

Additional data of a more “routine” characterization nature is described in Section 6.

5.1 Preamp Settling

This concern addresses the effects of the (unavoidable) reset clock feedthrough in the video signal. Ground testing shows some variability in the recovery time of this feature because of non-ideal behavior in the external preamp that is attached to the CCD enclosure. This preamp behavior cannot be changed by the ACS-R hardware, which must be made to accommodate an expected range of variation.

The purpose of this adjustment is to maintain proper CCD behavior while reducing the magnitude of the reset gate (RG) voltage. As this voltage is reduced, the feedthrough is reduced. The desire is to reduce this to a level that does not run the external preamp into saturation, from which it could potentially recover in a strange way. Ground testing shows that this is possible, and in all likelihood, we will use the ground test derived RG setting as the nominal.

Quantifying the effects of clock feedthrough into the output video voltage for the on-orbit case is the primary reason why Oscilloscope Mode was designed into the CEB-R. This mode routes the video signal directly into the SIDECAR ASIC, which then samples it at high speed (4 MHz) to provide voltage vs. time for the video signal within a pixel time (22 usec nominal, 88 samples per pixel). The current implementation is described elsewhere (“O-Scope Design Concept: Preliminary Discussion and Review”, Raphael Ricardo, Powerpoint, undated but sent March 6, 2008). Also see the Teledyne Imaging Sensors Flight Assembly Code Drop 2.7 Design and Operations Manual (or later revisions).

The RG test should ideally be run after every optimization cycle. It is possible that changing other clock voltages and/or timing patterns will have an effect on the optimal RG value. However, it is probably fine to run it once at the start of the optimization cycle, once at the end, and maybe one more time near the middle, since data requirements are fairly extensive.

5.1.1 Data Required

By default, these data will be taken with the Dual-Slope Integrator unless early on-orbit testing indicates that a switch to Clamp-and-Sample is desirable. With appropriate coding, a simple realtime command could be used to effect the change to Clamp-and-Sample, if necessary.

The gain of the CCD should be determined during the ACS-R Functional Test in order to provide a current value for setting the intensity levels to use for these tests. In particular, the value of “full-well” in the tests below will need to be determined.

The required data here are pairs of Oscilloscope Mode and normal image data taken at 3 reset gate (RG) voltage levels (pre-failure setting, nominal from ACS-R ground testing, and one below nominal). The pre-failure setting is expected to be the highest voltage setting (12.0 V), and the alternate settings are intended to reduce the effects of RG clock feedthrough (8.0 V nominal and 7.0 V below-nominal). The main performance parameters will be noise, full-well level, and gain. The video signal should be sampled at “no light” levels to determine the noise. The full-well level can be estimated using a near-full-well illumination frame and checking the output voltage achieved for, say ~0.9 of the expected full-well from pre-failure experience. The gain is not expected to change significantly, and can be determined at a particular RG value using at least one illuminated level around ~0.25 full-well for these measurements. The illuminated level should have a fairly well understood illumination intensity so that the gain can be estimated to ~10% accuracy based on absolute flux alone. We do not expect to need a full photon transfer gain calibration for each of these measurements if, as we expect, the light level is well understood. However, two frames of the illuminated data are requested for an independent check.

It is also possible for large changes in RG may affect the charge transfer efficiency of the final shift in the serial shift register. This will be investigated through lab tests and the results will inform the final implementation of this test.

This test is expected to span all reasonable parameter space for the RG determination. At any particular setting of the other configurable parameters, the desire is for this test to come up with the optimal RG setting.

There are Oscilloscope Mode and “normal” image data for each of the settings. The normal data are expected to be 512 x 512 subarrays to minimize time and data volume. All four output amplifiers need to be sampled, therefore there are four actual frames per setting since the subarray readout mode only reads out through one of the four amplifiers. In the table below, the number of frames is counted, assuming that four frames is the minimum number needed to read out through all four amplifiers.

This requires a total of 9 Oscilloscope Mode frames (one for each RG setting and illumination level), 3x4 subarray dark frames using the integrator (one for each RG setting), 2x3x4 subarray image frames using the integrator at ~0.25 full-well illumination (one for each RG setting), and 2x3x4 normal subarray frames using the integrator at ~0.9 full-well illumination (one for each RG setting). The illuminated frames are doubled up to allow for estimating the gain at each of the two intensity levels used. This test

requires a total of 9 Oscilloscope Mode frames and 60 normal subarray frames per execution.

Note that only the RG high rail is adjusted for this test. The low rail remains at the normal 0.0 V setting (within 1 DAC count).

Setting	Type	RG High Rail Setting (Volts)	Illumination (fraction of full-well)	Number of Frames
1	Oscilloscope	12	0	1
2	Normal	12	0	1x4
3	Oscilloscope	8	0	1
4	Normal	8	0	1x4
5	Oscilloscope	7	0	1
6	Normal	7	0	1x4
7	Oscilloscope	12	~0.25	1
8	Normal	12	~0.25	2x4
9	Oscilloscope	8	~0.25	1
10	Normal	8	~0.25	2x4
11	Oscilloscope	7	~0.25	1
12	Normal	7	~0.25	2x4
13	Oscilloscope	12	~0.9	1
14	Normal	12	~0.9	2x4
15	Oscilloscope	8	~0.9	1
16	Normal	8	~0.9	2x4
17	Oscilloscope	7	~0.9	1
18	Normal	7	~0.9	2x4

At the end of this test, the RG setting shall be put back to the Nominal setting of 8.0 V so that subsequent tests will use this nominal setting.

Adjustments to the RG High clock rail are made using the JCCDCLK macro.

The RG High clock rail settings used for this test are most naturally interpreted as absolute values. We are not trying to span a range of values around a nominal. These absolute values are expected to have specific “threshold” effects that are being investigated.

5.1.2 Intended Use Of The Data

The collected data will be used to generate noise, full-well level, and gain estimates. Note that these need not be absolute, and can be measured relative to, say, the nominal settings of RG.

After these data are collected, the final reset gate voltage can be determined. The intent is then to use the selected RG voltage by setting it at the next available realtime command window. Subsequent optimization runs will all use the newly selected RG voltage.

The timing pattern table entries may also be modified as a result of this test.

5.1.3 Analysis Tools Required

Analysis routines should determine the gain and full-well level figures-of-merit based on the normal image readout frames for each of the RG settings. The Oscilloscope Mode data will be examined visually, and should be easy to associate with these figures-of-merit. A tool that plots selected Oscilloscope Mode data with the figures-of-merit (noise [e^- RMS], gain [e^-/ADU], and extrapolated full-well level [e^-]) would be convenient.

It is expected that normal STScI analysis to provide gain, noise, and full-well can be used to address these analysis needs. Informal estimates show that this represents about 1 hour of elapsed analysis time after the data are received. This estimate should be refined to inform the scheduling of detailed activities during the Optimization Campaign.

5.2 Clock Feedthrough

When any of the clocks for the CCD change state, there may be significant capacitive coupling from those clocks into other clocks and/or the output signal. The coupling into other clocks is controlled by design, and to some extent by varying phasing and clock rail levels. There is not much else that can be done since most of this is internal to the CCD.

The coupling into the output can affect accuracy because of settling time in the downstream preamp and video electronics. The degree of this coupling is controlled in much the same way as above, but the video processing timing needs to be adjusted to accommodate the coupled waveforms. In particular, where feedthrough and settling is dominant, we certainly want to be in an “ignore” state rather than a “sample” state for the signal.

The clocks that affect the output voltage the most (the three phases of the serial clocks S1, S2, S3, and the summing well SW) will be adjusted, and the effects observed in Oscilloscope Mode, so that the timing pattern can be optimized to minimize the feedthrough effects while maintaining good performance. (The reset gate, RG, clock is treated separately in Section 5.1.) The serial clocks (S1, S2, S3) share common rails so that these will be treated as one “clock” for the purposes of the voltage adjustments for this test. There are thus a total of 4 voltages to optimize:

1. Serial clock high rail
2. Serial clock low rail
3. Summing well high rail
4. Summing well low rail

It is possible that dramatic changes of the serial clocks and summing well can change the full-well level and the serial charge transfer efficiency. This will be investigated

through lab tests to determine an adjustment range that is unlikely to affect these important performance parameters.

5.2.1 Data Required

The video signal should be sampled at “no light” levels and at least one illuminated level around half full-well for these measurements. The illumination level is not critical, and can be estimated based on pre-failure performance.

This requires a total of 9 dark and 9 illuminated Oscilloscope Mode frames. In the first pair of frames, the clock rails will be at their nominal voltages. In subsequent frames, the high and low rails of one of the clocks will be adjusted away from its nominal. Filling in all possible variations for the voltages being adjusted leads to the following table. Nominal is the value determined best by ground testing and encoded into the preplanned SMS commanding (+5 V for the high rails, and -6 V for the low rails). We test +/- 1 V deviations from these nominal values. These absolute values can be encoded in the SMS as a nominal voltage and a deviation magnitude (in this case, 1 V). Only Oscilloscope Mode frames are required. The grouping of the frames is not important and can be adjusted for best efficiency.

Frame	Illumination (fraction of full-well)	Serial Clock High Rail (V)	Serial Clock Low Rail (V)	Summing Well High Rail (V)	Summing Well Low Rail (V)
1	0	+5	-6	+5	-6
2	~0.5	+5	-6	+5	-6
3	0	+5+1	-6	+5	-6
4	~0.5	+5+1	-6	+5	-6
5	0	+5-1	-6	+5	-6
6	~0.5	+5-1	-6	+5	-6
7	0	+5	-6+1	+5	-6
8	~0.5	+5	-6+1	+5	-6
9	0	+5	-6-1	+5	-6
10	~0.5	+5	-6-1	+5	-6
11	0	+5	-6	+5+1	-6
12	~0.5	+5	-6	+5+1	-6
13	0	+5	-6	+5-1	-6
14	~0.5	+5	-6	+5-1	-6
15	0	+5	-6	+5	-6+1
16	~0.5	+5	-6	+5	-6+1
17	0	+5	-6	+5	-6-1
18	~0.5	+5	-6	+5	-6-1
19	0	+5	-6	+5	-6

At the end of this test, the four clock rail settings shall be put back to the nominal settings of +5 V for the high rails and -6 V for the low rails so that subsequent tests will use this nominal setting.

It is possible that during ground testing or even early SMOV testing, we may determine that a more complicated combination is desirable. In this case, we will replace some of these simple combinations. In other words, this structure and amount of data should be planned, keeping in mind the possibility that we may want to change the exact combinations tested with these 18 frames.

Adjustments to the clock rails are made using the JCCDCLOCK macro.

5.2.2 Intended Use Of The Data

The exact timing adjustments that need to be made will depend on the data returned from this test. These adjustments will be based on inspection of the Oscilloscope Mode data to ensure that the timing that is implemented will minimize the effects of the feedthrough.

The adjustments are intended to be sent by realtime commanding to patch the 88 words of the timing pattern table. Adjustments will be made using the JLDASIC1 macro.

Once the timing pattern is established, it will be used for all subsequent tests.

5.3 Bias and Clock Voltage Optimization

Each CCD has an optimal setting for its biases and clock rails. The biases mostly affect noise and full-well level, whereas the clock rails affect CTE.

The nominal voltages used for the flight CCDs (the last time they were operable) provide a good starting point for the CEB-R, and will be the default values at launch. However, since these CCDs would have suffered several years of radiation damage, it is possible (and likely) that the optimal settings are now different. The differences are not expected to be large, so it is possible that gathering a modest set of performance data for a range of parameters will allow for selecting the optimal set.

5.3.1 Data Required

For the biases, the data shall be taken in both the Dual-Slope Integrator and Clamp-and-Sample modes. The voltages that need to be examined are:

- CCD_VLG (the CCD "last gate" voltage)
- CCD_VOD (the drain on the reset transistor)
- CCD_VDD (the drain on the output transistor)

These can be varied simultaneously on the two CCDs. Because we want to determine the noise, full-well level, and gain, the illumination strategy is very similar to that in Section 5.1. Two illumination frames are used to estimate the gain changes for each setting. Normal images using subarrays of 512 x 512 pixels will suffice. However, since all four amplifiers need to be sampled, there will be four frames per image, one for each output amplifier.

Setting	Illumination (fraction of full-well)	CCD_VOD	CCD_VDD	CCD_VLG	Number of Frames
1	0	15.0	26.5	-4.0	1x4
2	~0.25	15.0	26.5	-4.0	2x4
3	~0.9	15.0	26.5	-4.0	2x4
4	0	15.0	28.0	-4.0	1x4
5	~0.25	15.0	28.0	-4.0	2x4
6	~0.9	15.0	28.0	-4.0	2x4
7	0	16.0	28.0	-4.0	1x4
8	~0.25	16.0	28.0	-4.0	2x4
9	~0.9	16.0	28.0	-4.0	2x4
10	0	16.0	27.5	-4.0	1x4
11	~0.25	16.0	27.5	-4.0	2x4
12	~0.9	16.0	27.5	-4.0	2x4
13	0	14.0	26.5	-4.0	1x4
14	~0.25	14.0	26.5	-4.0	2x4
15	~0.9	14.0	26.5	-4.0	2x4
16	0	14.5	26.5	-4.0	1x4
17	~0.25	14.5	26.5	-4.0	2x4
18	~0.9	14.5	26.5	-4.0	2x4
19	0	14.0	25.0	-4.0	1x4
20	~0.25	14.0	25.0	-4.0	2x4
21	~0.9	14.0	25.0	-4.0	2x4
22	0	15.0	26.5	-5.0	1x4
23	~0.25	15.0	26.5	-5.0	2x4
24	~0.9	15.0	26.5	-5.0	2x4

At the end of this test, the biases shall be reset to those for Setting 1 so that subsequent tests will use this nominal setting.

This table represents 8x5x4=160 frames of 512 x 512 subarray data. The precise voltage settings may be further refined based on ground testing.

For the clocks, only the serial and parallel clock rails need to be checked. (The pixel-readout clocks are checked in Section 5.1.) Note that this test is not the same as the one in Section 5.2, so the Serial Clock Rail tests here are not the same as the ones done there. Because of the data volume, the clocks shall be tested in only the Dual-Slope Integrator mode. If on-orbit testing shows that a switch to the Clamp-and-Sample mode is required, then a rapid SMS edit will be needed.

- Serial Clock High Rail
- Serial Clock Low Rail
- P1/P2 Parallel Clock High Rail
- P1/P2 Parallel Clock Low Rail
- P3 Parallel Clock High Rail

P3 Parallel Clock Low Rail

Here, we are interested in CTE, so it is necessary to take EPER frames. These are less efficient, mainly because the existing timing only reads out through one amplifier on each CCD, and subarrays are not supported. In this case only one amplifier on each CCD needs to be monitored since these clocks are not output-specific. Other parameters of interest are noise and full-well level.

Nominal is the value determined best by ground testing and encoded into the preplanned SMS commanding (Frames 1 to 3). We test ± 1 V deviations from these nominal values. These absolute values can be encoded in the SMS as a nominal voltage and a deviation magnitude (in this case, 1 V).

Frame	Illumination (fraction of full-well)	Serial Clock High Rail (V)	Serial Clock Low Rail (V)	P1/P2 High Rail (V)	P1/P2 Low Rail (V)	P3 High Rail (V)	P3 Low Rail (V)	Number of Frames
1	0	+5	-6	+3	-8	+6	-6	1
2	~0.25	+5	-6	+3	-8	+6	-6	1
3	~0.75	+5	-6	+3	-8	+6	-6	1
4	0	+5+1	-6	+3	-8	+6	-6	1
5	~0.25	+5+1	-6	+3	-8	+6	-6	1
6	~0.75	+5+1	-6	+3	-8	+6	-6	1
7	0	+5-1	-6	+3	-8	+6	-6	1
8	~0.25	+5-1	-6	+3	-8	+6	-6	1
9	~0.75	+5-1	-6	+3	-8	+6	-6	1
10	0	+5	-6+1	+3	-8	+6	-6	1
11	~0.25	+5	-6+1	+3	-8	+6	-6	1
12	~0.75	+5	-6+1	+3	-8	+6	-6	1
13	0	+5	-6-1	+3	-8	+6	-6	1
14	~0.25	+5	-6-1	+3	-8	+6	-6	1
15	~0.75	+5	-6-1	+3	-8	+6	-6	1
16	0	+5	-6	+3+1	-8	+6+1	-6	1
17	~0.25	+5	-6	+3+1	-8	+6+1	-6	1
18	~0.75	+5	-6	+3+1	-8	+6+1	-6	1
19	0	+5	-6	+3-1	-8	+6-1	-6	1
20	~0.25	+5	-6	+3-1	-8	+6-1	-6	1
21	~0.75	+5	-6	+3-1	-8	+6-1	-6	1
22	0	+5	-6	+3	-8+1	+6	-6+1	1
23	~0.25	+5	-6	+3	-8+1	+6	-6+1	1
24	~0.75	+5	-6	+3	-8+1	+6	-6+1	1
25	0	+5	-6	+3	-8-1	+6	-6-1	1
26	~0.25	+5	-6	+3	-8-1	+6	-6-1	1
27	~0.75	+5	-6	+3	-8-1	+6	-6-1	1

At the end of this test, the biases shall be reset to those for Frame 1 so that subsequent tests will use this nominal setting.

The total amount of data described in this table is $9 \times 3 = 27$ EPER frames.

Adjustments to the biases are made using the JCCDBIAS macro.

Adjustments to the clock rails are made using the JCCDCLK macro.

5.3.2 Intended Use Of The Data

The collected data will be analyzed for noise and gain (biases) and noise and CTE (clocks, assuming nominal gain) and the best variations identified.

Once the optimal voltages are established, they will be used for all subsequent tests.

It is expected that normal STScI analysis to provide gain, noise, CTE, and full-well can be used to address these analysis needs. Informal estimates show that this represents about 12 hours of elapsed analysis time after the data are received. This estimate should be refined to inform the scheduling of detailed activities during the Optimization Campaign.

5.4 Parallel Clock Settling

In order to maintain the cleanest clock edges and minimize clock crosstalk in the CEB-R, the output driver rise and fall times are controlled by RC time constants. These are somewhat slower than the original CEB implementation. The edge speeds are not expected to have a significant impact on the parallel shift CTE. However, the slower speed does reduce somewhat the amount of time that each of these clocks spend at the clock rails. There may be a CTE impact from this reduced time.

5.4.1 Data Required

The easiest way to determine if the normal parallel clock timing is adequate is to compare two well-illuminated EPER frames taken with different parallel shift delays. The parallel shift delays are adjusted by patching special ASIC memory locations (within the timing file) after the timing file is loaded. This may be unnecessarily complicated unless we see a problem.

If we assume that the pre-failure parallel CTE is the best that can be achieved, it is possible to just compare the measured CTE to the predicted CTE based on previous performance and the additional time on-orbit. This will provide a means to assess whether we are “as good” as before, but not the means to achieve any potential improvement. The data needed for this comparison will already be collected as a part of the normal Performance Summary runs to be described later.

5.4.2 Intended Use Of The Data

The data will be used to estimate the (parallel) CTE of the CCD devices.

If we find that the parallel CTE reported by the Performance Summary is significantly different from the pre-failure experience extrapolated to the current time, then discussions will need to be held to determine if adjusting the parallel shift delay is advisable. Note that increasing the parallel shift delay will increase the frame readout time (by a small amount).

5.5 Ground Noise

The grounding system for the CEB has certain features that may be of concern. In particular, there is a single-point power ground in the CEB backplane that, in the old CEB configuration, was probably benign. In the CEB-R, we are trying to backpower the HRC CEB through the original power buses. This makes all the return currents, including the HRC currents, flow through the WFC CEB backplane. This ground loop could not be remedied by any features in the ACS-R design. We believe that the effects will be tolerable, and this is verified by ground testing. However, in the worst case on orbit, we may need to power down the HRC CEB.

Because of this concern, some characterization of noise with and without the HRC CEB powered on is desirable. Very little data is required, perhaps a bias frame with and without the HRC CEB on will do. This could be done during the Optimization Campaign, or is perhaps more natural afterwards as a part of normal instrument calibration. The other optimization data described in the above sections would ideally be taken with the HRC CEB turned off (i.e., no backpowering) to isolate any potential effects from ground noise. However, since the ACS-R needs to operate in an environment where everything is on, such an isolated test may only be of academic interest, so it is arguable that we should run the optimization tests with as many things on as is “normal”. In the event that the WFC and HRC are not “compatible” in this manner, the HRC would probably be used in “campaign mode”.

5.6 Science Data Transmission Timing

Ground testing has determined that the transmission of the serialized science data from the CEB-R to the MEB is a significant source of noise that couples back into the video inputs. This is a direct consequence of copying the CEB-to-MEB interface faithfully in the CEB-R implementation. This same effect was noticed and needed attention in the WFC3 (instrument) CEB and MEB, which is of a similar design.

The CEB-R science data transmission rate is settable by the CEB-R science data rate prescaler that can set the rate to $4 \text{ MHz} / (N+1)$, where the prescaler value N is between 0 and 3, inclusive. The previous ACS CEB operated only at 1 MHz, and the original intent was to maintain this practice.

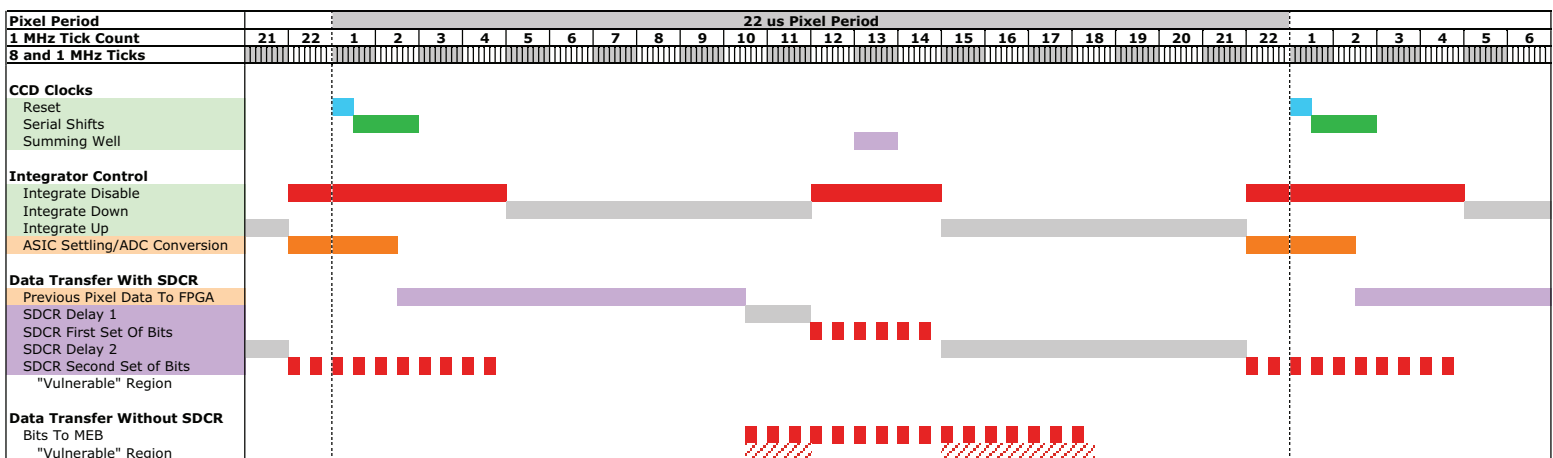
At 1 MHz, a 16-bit quantity requires 16 μs to transmit. The pixel time is 22 μs . Thus, roughly 0.75 of a pixel integration time is potentially corrupted by noise coupling from the science data transmission. By increasing the rate to 2 MHz, this ratio can be reduced by a factor of 2 to 0.375, or 8 μs of transmission time. Ground testing has shown that a significant noise reduction is achieved in this case.

This noise has been significantly reduced by adding the differential optoisolator drive to the flight CEB-R. Ground testing after this change shows that it is very effective, and reduces the coupling so that the change in noise between a 1 MHz data transmission rate and 2 MHz rate is less than 0.1 electrons (i.e., negligible). Nevertheless, the flight default will be set to 2 MHz for margin, if possible. Because this configuration has not been tested with the on-orbit ACS MEB, the SM4 AT/FT will be performed with the previously used 1 MHz rate. A test will be scheduled early during SMOV (before the Optimization Campaign) to verify that the 2 MHz rate operates as expected. It is also possible to change the rate to an intermediate 1.333 MHz if the 2 MHz rate does not work. If 1.333 MHz is the rate we decide to run at (for whatever reason), the details of how to perform this test may have to change.

The following diagram illustrates the key timing relationships relative to data output. It assumes a 2 MHz CEB-R to MEB data transmission rate, and a nominal timing pattern for the Dual-Slope Integrator.

Each pixel takes 22 μ s to read out, and the pixels are read out in sequence (no dead time between pixels). The timing for each pixel is shown in the middle portion of the diagram, between the vertical dotted lines. Portions of the previous and next pixels are shown because the data output for a pixel overlaps the video processing for the next pixel.

The color coding of first column shows how the timing parameter is adjusted. Light green is controlled by the readout timing pattern. Orange is an internal ASIC register (one set per timing pattern). Purple is the Science Data Control Register (SDCR) in the CEB-R FPGA.



The video signal presented to the CEB-R is controlled by the CCD Clocks. The Reset clock resets the output amplifier to a Reference Voltage. After this reset, the serial clocks are activated to shift the charge to the input of the Summing Well (but it does not go into the Summing Well until the Summing Well clock is activated). During this period, the video output voltage is a large transient from the Reset Clock feedthrough, as well as the Serial Clock feedthrough, settling eventually to the Reference Voltage we

want to measure. This period lasts nominally 4 μs from the start of the pixel, as measured by the rising edge of the Reset clock.

From 5 to 11 μs , the integrator integrates the Reference Voltage “down” to arrive at a noise-reduced measurement of this voltage.

The integrator is then disabled, and the Summing Well clock activated to transfer the charge to the capacitor at the input of the output amplifier. Call the resulting voltage the Signal Phase Voltage. The change in voltage from the Reference Voltage to the Signal Phase Voltage is proportional to the amount of charge for the pixel. There is a small feedthrough from the Summing Well clock in the video output during this time, and we allow 3 μs for this to settle (and to minimize crosstalk, which we learned from ground testing).

From 15 to 21 μs , the integrator integrates the Signal Phase Voltage “up”. At the end of this period, we effectively have a time-averaged measurement of the Signal Phase Voltage minus the Reference Voltage.

From 21 to 22 μs , the integrator is disabled (making the voltage at its output static), and the integrator output is presented to the ASIC for sampling and digitization. The exact timing of the ADC conversion is settable via the ADC Sample Hold Delay timing control register in the ASIC.

After conversion, the data are sent from the ASIC to the FPGA. There is no evidence that this internal transmission within the CEB-R causes any undesirable effects (like increased noise or crosstalk). The exact timing of this transmission is controllable via the Data Out Delay control register in the ASIC.

After the FPGA receives this data, it serializes it for transmission to the MEB. This is the transmission that had been observed to couple into the video signal. Without the SDCR, or at the power-up value of the SDCR, the timing of the transmission is as shown in the “Data Transmission Without SDCR” lines. During the central 1 μs of this period, the integrator is disabled, so is insensitive to any noise. However, for the majority of this period (7 μs), any noise generated by data transmission can couple into both the integrate down and integrate up phases of the next pixel. These “Vulnerable Periods” are shown in the diagram underneath the timing shown for the 16 bits being transmitted.

The concept of the Science Data Control Register is to use the fact that the FPGA has more flexibility than the ASIC in controlling the science data transmission. In fact, the FPGA is often called a “translator FPGA” that goes between the ASIC packetized transmission scheme and the external interface. This register controls FPGA circuitry that can split the 16-bit transmission into two parts (of 16-bit total length, but selectable lengths for the parts), and also an arbitrary delay before the transmission of the first part, and another delay for the second part. In this manner, the transmission can be tailored to look something like what is shown for the “Data Transfer With SDCR” case. We can transmit some of the bits during the Summing Well integrator disabled period, and the rest of them during the next Reset and Serial Shift period.

The default readout timing pattern for flight is as described above, and in theory, provides exactly the right amount of integrator-disabled time to transmit all the bits at a 2 MHz bit rate.

For any particular timing pattern, calculation and ground testing can be used to determine the best setting for these parameters. Nevertheless, it would be prudent to check the on-orbit system to ensure that the selected values are optimum.

Note that we ignore the “output channel enable” bits in the Science Data Control Register. These are used only for ground testing, and are not expected to be useful on-orbit.

5.6.1 Data Required

By default, these data will be taken with the Dual-Slope Integrator unless early on-orbit testing indicates that a switch to Clamp-and-Sample is desirable. With appropriate coding, a simple realtime command could be used to effect the change to Clamp-and-Sample, if necessary.

The data required are dark frames for noise determination. Subarrays of 512 x 512 are acceptable. To minimize data volume, only Output B will be used for this test since it has the lowest pre-failure noise. Since this is purely a data transmission adjustment, the gain properties of the CCD will be constant, so only the noise needs to be monitored during the test.

The parameters in the table below (Split, Delay 1, Delay 2) are expected to be set to the pre-launch determined values in the planned commanding. Split is called the “Number of bits in first part” in the FPGA document. Delay 1 is the “Pretransmit delay”, and Delay 2 is the “Intercommand delay”. The numbers below are *increments* that are intended to show the change from the initial values at launch. “Split” determines the number of bits in the first transmission group of bits, “Delay 1” is the delay of the first group (starting right after the ASIC sends the entire set of packetized data for a pixel), and “Delay 2” is the delay for the second group (starting right after the first group is sent). The idea is to scan 4 steps in delay on either side of the initial values for both delays, and then to change the split by +/-1 bit. Some of these are expressed as a sum of two numbers to make the derivation a little more obvious. The concept is to first move the first group of bits by +/-1 bit time (+/- 4 counts in the delay registers). Because the Delay 2 starts from the end of the first group of bits, it needs to compensate for the Delay 1 setting in order to keep the second group of bits invariant. We then move the second group of bits around by the same +/- 4 counts amount. Then we add a bit to the first group and do the same thing after recentering the first and second groups around the same average time (thus the “-2” values in all the Delay 1 settings and “+4” in the Delay 2 settings for these cases). Finally, we remove a bit from the first group and do it again. We assume that the nominal settings of this register will look something like the “Data Transfer With SDCR” case shown in the diagram above.

Frame	Split	Delay 1	Delay 2	Comments
1	+0	+0	+0	Nominal Split
2	+0	+1	-1	Move first group of

3	+0	+2	-2	bits +/- 1 bit time	
4	+0	+3	-3		
5	+0	+4	-4		
6	+0	-1	+1		
7	+0	-2	+2		
8	+0	-3	+3		
9	+0	-4	+4		
10	+0	+0	+1		Move second group of bits +/- 1 bit time
11	+0	+0	+2		
12	+0	+0	+3		
13	+0	+0	+4		
14	+0	+0	-1		
15	+0	+0	-2		
16	+0	+0	-3		
17	+0	+0	-4		
18	+1	+0-2	+0+4	Nominal+1 Split	
19	+1	+1-2	-1+4	Move first group of bits +/- 1 bit time (one more bit in first group)	
20	+1	+2-2	-2+4		
21	+1	+3-2	-3+4		
22	+1	+4-2	-4+4		
23	+1	-1-2	+1+4		
24	+1	-2-2	+2+4		
25	+1	-3-2	+3+4		
26	+1	-4-2	+4+4		
27	+1	+0-2	+1+4	Move second group of bits +/- 1 bit time (one more bit in the first group)	
28	+1	+0-2	+2+4		
29	+1	+0-2	+3+4		
30	+1	+0-2	+4+4		
31	+1	+0-2	-1+4		
32	+1	+0-2	-2+4		
33	+1	+0-2	-3+4		
34	+1	+0-2	-4+4		
35	-1	+0+2	+0+4	Nominal-1 Split	
36	-1	+1+2	-1+4	Move first group of bits +/- 1 bit time (one less bit in the first group)	
37	-1	+2+2	-2+4		
38	-1	+3+2	-3+4		
39	-1	+4+2	-4+4		
40	-1	-1+2	+1+4		
41	-1	-2+2	+2+4		
42	-1	-3+2	+3+4		
43	-1	-4+2	+4+4		
44	-1	+0+2	+1+4	Move second group of bits +/- 1 bit time (one less bit in the first group)	
45	-1	+0+2	+2+4		
46	-1	+0+2	+3+4		
47	-1	+0+2	+4+4		
48	-1	+0+2	-1+4		
49	-1	+0+2	-2+4		
50	-1	+0+2	-3+4		

51	-1	+0+2	-4+4	
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This is a total of 51 normal dark frames using a 512 x 512 subarray.

Adjustments to the Science Data Control Register are made using the JFPGASDC macro.

5.6.2 Notable Dependencies

If the timing pattern tables are changed so that the time separation between the Reset Gate and Summing Well phases is changed, then the default values of this register may need to change. It is not expected that we will be changing this time separation because the goal is to get equal sampling on the reset and signal video phases. Nevertheless, it is a possibility and should be noted. If we change this time separation, then the “nominal” values assumed for this test may change. Either we can figure out how to deal with this via a late-notice SMS change, or we have to span a larger range of settings in the table here.

5.6.3 Intended Use Of The Data

Generate plots showing the location of the optimum setting for low noise. If the optimum is not at the pre-flight selected values, generate realtime commands to correct.

6 Operational Concept

Based on discussion with the operations community, we have allocated 3 weeks of elapsed time during SMOV to complete the optimization process. This section discusses the things that need to happen during this time, and the concept of how it could be done.

There is a strong desire to minimize the amount of time spent during this Optimization Campaign. If at all possible, the detailed planning should allow for truncation of this campaign if we can determine early on that we have achieved our goals. From initial discussions, it appears that if the three weeks are lined up with a normal calendar week, then we can make last-minute changes to the SMS for a particular week up to the Wednesday of the previous week. Realistically, the option here is for deleting the last week of this three week period, since it seems unlikely that we will be fine after only the first few days of the planned Optimization Campaign.

6.1 Types Of Data Acquisition

The data that need to be taken fall into one of the following three categories.

6.1.1 Span Parameter Space

At the recommendation of the accumulated operations experts, we have tried to lay out as many things as we can that “span parameter space”. This allows for running one, possibly complex, set of data acquisitions that, when analyzed, will determine the optimal parameters to use. Some of the measurements in Sections 5.1, 5.3, and 5.6 have been cast into this model.

6.1.2 Individual Pixel Optimization

Nevertheless, there are some optimizations, namely the detailed timing adjustments for feedthrough optimization, that simply have too many parameters to span all parameter space. For these, an iterative approach is proposed. Data would be collected at a frequent interval and analyzed. The results will cause some combination of parameters to become interesting. New values for these will then be uplinked and used as the next set of parameters for the next data collection run. The measurements in Section 5.2 are of this type.

6.1.3 Performance Summary

After we believe we have the instrument in a fiducial state, it would be necessary to gather some basic information about the instrument performance in the main performance parameters:

1. Noise [e^- RMS]
2. Gain [e^- /ADU]
3. CTE (parallel and serial)
4. Linearity and Full-well Level [e^-]
5. Crosstalk

Several discussions have taken place to understand the images that will be required to provide the necessary information. Here we provide only the guidelines for what will be needed. The detailed image list will be left to the detailed planning that will need to take place.

- A. Illuminated and dark data will be required. The illuminated data should be taken so that they have accurate enough illumination ratios to use for determining linearity.
- B. There may be benefit to acquiring two images per signal level in order to separate the effects of CTE from gain variations. The two images can be used to estimate the gain at the illumination level used.
- C. The data could be taken for a subarray of the CCDs as long as this subarray is representative of device performance.
- D. All four output amplifiers should be used for noise, gain, linearity, full-well, and crosstalk.
- E. CTE measurements can sample only one output amplifier in each CCD if this is more efficient.
- F. Both the integrator and clamp-and-sample video chains should be exercised. If the integrator is working well, one could make a policy decision to defer clamp-and-sample optimization. The optimizations will likely be different for these two modes. One possibility is to plan to do both for the first week, and decide soon after the baseline performance test whether we can scale back to just the integrator (if the initial data look promising) for the second and third weeks.
- G. Half-speed mode should be exercised if it is available for SMOV, at least for a subset of these runs (for example, at the beginning, middle, and end of the Optimization Campaign). Even if there is no plan to support science observations in this mode, it (the half-speed mode) has been demonstrated to be a good diagnostic during ground testing for separating noise contributions from different effects.

The crosstalk measurement has taken on a new urgency because of a sensitivity discovered during ground testing. This mostly affects the DSI video chain (i.e., does not seem to affect the C&S chain). Minor changes in the Summing Well timing has been found to change the channel A-to-B and C-to-D crosstalk by over an order of magnitude. The optimal setting for ground testing can be determined, but the on-orbit case may depend in detail on the CCD and External Preamp, and may need optimization. The Performance Summary test already provides the information necessary to assess the crosstalk, and this test is performed quite regularly, so the crosstalk optimization will be performed every iteration. The crosstalk analysis will likely need to use a dark frame and the hot pixels in the detectors.

6.1.4 Oscilloscope Mode Readout Of Internal Signals

The intent of this acquisition is to check the relative phasing of the internal ASIC signals to the incoming video signal. It is primarily an engineering test to ensure that the desired timing is achieved. For the default timing, this is probably unnecessary since it has been extensively used and characterized during ground testing. The primary

benefit of these data is to ensure that the timing patterns modified (in realtime) during SMOV produce the expected timing so that the resulting data are properly interpreted.

This acquisition selects an internal signal from the ASIC to be monitored together with three quadrants of true video signals. We will plan for each of these runs to provide 13 Oscilloscope Mode frames, each with preset configuration as determined by the SMS that monitors a different internal signal. The first Oscilloscope Mode frame will not specify the Oscilloscope Mode configuration register values in order to allow realtime commanding to specify an unanticipated need.

These Oscilloscope Mode frames should all be illuminated to ~0.5 full-well in order to reveal the full dynamics in the video signal within a pixel. If inconvenient, dark frames should be fine since the Oscilloscope Mode pixel list will contain pixels with large signals.

The configuration for the 4 Oscilloscope Mode Channels are specified in the following table. "Raw Video" is the video signal after the first differential amplifier in the CEB-R. It is the signal that represents what is coming out of the CCD. There is one Raw Video signal for every CCD output amplifier (A through D). See Section 4.5 for warnings about these signals in FM1. The "DSI" and "C&S" entries are the Dual-Slope Integrator and Clamp-and-Sample processed outputs as they are seen at the ASIC inputs. These are normally the signals that get sampled to produce the image data. Again, there are four of these signals, one for each CCD output amplifier. Not all versions of the internal clocks are checked in this scheme. In cases where we only need to check one of them, they are marked with A or B.

Frame	Channel A	Channel B	Channel C	Channel D (ASIC Internal Signal Sampled)
1	Use the current value specification in ASIC memory that may have been patched using realtime commanding.			
2	Raw Video A	Raw Video B	DSI B	Reset Gate
3	Raw Video A	Raw Video B	DSI B	Summing Well B
4	Raw Video A	Raw Video B	DSI B	Serial Clock 1 B
5	Raw Video A	Raw Video B	DSI B	Serial Clock 2 AB
6	Raw Video A	Raw Video B	DSI B	Serial Clock 3 B
7	Raw Video A	Raw Video B	DSI B	Integrator Input Clamp
8	Raw Video A	Raw Video B	DSI B	Integrator Enable
9	Raw Video A	Raw Video B	DSI B	Integrator Reset
10	Raw Video A	Raw Video B	DSI B	Integrator Polarity
11	Raw Video A	Raw Video B	DSI B	Integrator Output En X
12	C&S B	Raw Video B	C&S C	Clamp-and-Sample Input Clamp
13	C&S B	Raw Video B	C&S C	Clamp-and-Sample Clamp/Sample

At the end of this acquisition, the Oscilloscope Mode configuration register values should be reset to their default values for monitoring the four CCD output amplifier Raw Video signals.

The first 11 frames are run in Dual-Slope Integrator mode. The last two frames are in Clamp-and-Sample mode.

The Oscilloscope Mode configuration register values corresponding to these cases are provided by Teledyne Imaging Sensors. They are changed using macro JWOSCPRM.

6.2 Types of Realtime Commanding

Realtime commands may or may not be required during the Optimization Campaign. However, the nature of this plan is that unless everything is perfect when we get to orbit, the data gathered are intended to result in realtime commands that will be used to improve the performance of the hardware. The SMS may also be used for longer-range and/or more permanent changes, but we are assuming that there is a roughly 2 week lead time for this mechanism.

The operational scenario we envision will gather, on a repetitive basis, a predefined set of data that can inform adjustments to the hardware to improve some aspect of performance. Between these repetitions, there needs to be a realtime commanding window that adjusts the hardware parameters for the next iteration.

In the sections that follow, the types of realtime commands and their intended use are described.

6.2.1 Biases and Voltage Rails

These adjustments are straightforward CEB-R commands that affect the hardware immediately. Once set, they remain at their set values until the ASIC is reset (or powered down), or they are set to other values.

Use macros JCCDBIAS and JCCDCLCK to adjust these parameters.

6.2.2 Timing Pattern Table Adjustments

As discussed in Section 4.2, there are 44 words in ASIC memory that control the detailed pixel-level timing for each of the timing patterns. These 44 words are the bit patterns that control 16 clock lines, with each word representing 0.5 μ s of time (the pixel period is 22 μ s). These words are patched in ASIC memory, and are used to control the clocks when the timing files are loaded and run. They remain at their set values until the ASIC is reset (or powered down), or they are set to other values.

Use macro JLDASIC1 to adjust these parameters.

6.2.3 Science Data Control Register (SDCR)

This control register within the FPGA in the CEB-R controls the detailed timing of the transmission of the science data bits relative to the pixel readout timing (the period of time controlled by the 44 words of the Timing Pattern Table, as described in previous sections. It helps to place the transmission of the science data bits during times that are not critical to the video processing circuitry. Since the science data bits have been found to cause noise because of crosstalk back into the raw video signal, this is a noise reduction strategy.

This register can be written at any time to change its behavior immediately. It is best not to change it when science data transfers are occurring.

Use macro `JFPGASDC` to adjust these parameters.

6.2.4 Science Data Rate Prescaler

This register is an emulation of the one on the original CEB. It controls the rate at which the science data bits are transmitted from the CEB-R to the MEB. For noise control purposes, we want this to be the fastest speed possible, expected to be 2 MHz. The original CEB operated at 1 MHz.

The only time this would be changed in realtime is if we discover before SMOV that the 2 MHz does not work for the on-orbit hardware. We plan to use 2 MHz as the default for SMOV observations, and will revert to 1.333 MHz or 1 MHz if this proves to be a problem from a pre-SMOV test. Note that the desire is for there to be enough time to change the SMS as a result of any such testing, so that realtime commanding would not be required.

Use macro `JFPGACCR` to adjust this parameter.

6.2.5 Oscilloscope Mode Configuration Register

The Oscilloscope Mode Configuration Registers set the offsets and gains for the oscilloscope function, and the pixel locations to sample. They also enable selecting an internal clock to monitor in one of the four channels instead of the normal video signal for that channel.

These words are patched in ASIC memory, and are used to control the Oscilloscope Mode characteristics when that timing file is run. They remain at their set values until the ASIC is reset (or powered down), or they are set to other values.

Use macro `JWOSCPRM` to adjust these parameters.

6.2.6 SIDECAR ASIC Analog-to-Digital Conversion Timing Delays

There are two delays internal to the ASIC that may be useful to adjust. The first is the ADC Sample Hold Delay (ASIC register x410E) that controls the delay before the analog-to-digital conversion starts, relative to a fiducial point in the timing pattern. The second is the Data Out Delay (ASIC register x680F) that controls the delay between analog-to-digital conversion end and the sending of the data bits to the Timing Board FPGA. This overall function of this register is now a little redundant with the availability of the Science Data Control Register, but it controls the delay at a different interface (ASIC-to-FPGA instead of FPGA-to-MEB).

Use macro `JLDASIC1` to adjust these parameters.

6.2.7 Gains and Offsets

The CEB-R is expected to be run mostly using two gains, $\sim 1 \text{ ADU/e}^-$, and $\sim 2 \text{ ADU/e}^-$. Each gain setting may need its own offset adjustment to maximize the dynamic range that is sampled by the Analog-to-Digital converter. Because of non-ideal behavior

within the ASIC, the offset should be set so that the lowest signal value of interest (bias level) is around 2500 ADU for the Dual-Slope Integrator.

We may need to optimize the offsets during the Optimization Campaign for the gains that are used during this period. For other gains, the optimization is reserved for the extensive calibration period that follows the Optimization Campaign.

The offsets are commanded as an index into an internal ASIC table that controls the offset voltage. These table values can be patched if offset adjustments are required.

Use macros `JLDASIC1` and `JCCDGAIN` to adjust these parameters.

6.3 Sequence Of Events

Here is a rough timeline of the way the 3 weeks will be spent, using the nomenclature described above. The time estimates below are all TBR. They also assume nearly instantaneous access to the data.

The thinking days are a best guess at this point of the turnaround times for the analysis. There has been discussion of running the repeating pattern every day or every other day so that we can catch the next realtime uplink opportunity quickly should the analysis results be late. This is fine if the data volume can be supported, but is probably a little wasteful since the data being acquired are not insignificant. The list below is intended to convey the “requirement”, or at least our current concept of the requirement.

The pause after the first data taking exercise is intended to be longer than for subsequent iterations. The expectation is that the first run will require some more time to process and understand, so we should plan for it.

There has also been discussion of running an Oscilloscope Mode Readout during the post-EVA Functional Test. Such a precursor test would involve one dark and one illuminated (~0.5 full well) frame in Oscilloscope Mode, and would provide a useful heads-up for what to expect at the start of the Optimization Campaign.

There has been discussion as well of testing the 2 MHz science data transmission rate before the start of SMOV. The intent is that SMOV will use a default of 2 MHz. This is different from how the old CEB-MEB operated, which was at 1 MHz. Sometime before SMOV, a test could be run with the ASIC simulated data generator in the CEB-R to demonstrate that both the 1 MHz and 2 MHz rates work, and that they return the same data pattern.

The sections below describe the activities that are shown on the following chart of the 21 days allocated to CEB-R optimization.

We plan for an October 8, 2008 launch, for which we are informed that Iteration 1 will occur during a Friday (second to last day of an SMS).

Activity \ Day	Fr	Sa	Su	Mo	Tu	We	Th	Fr	Sa	Su	Mo	Tu	We	Th	Fr	Sa	Su	Mo	Tu	We	Th	Fr	Sa
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Iteration 1																							
Get baseline data																							
Optimize Preamp Feedthrough																							
Optimize Science Data Transmission Timing																							
Thinking Time 1																							
Iteration 2																							
Optimize Clock Feedthrough																							
Thinking Time 2																							
Iteration 3																							
Optimize Clock and Bias Voltages																							
Thinking Time 3																							
Iteration 4																							
Recheck Clock Feedthrough																							
Thinking Time 4																							
Iteration 5																							
Potential last iteration																							
Recheck clock feedthrough																							
Iteration 6																							
Get baseline data with Day 12 best-guesses																							
Repeat Iteration 1																							
Thinking Time 6																							
Iteration 7																							
Repeat Iteration 1																							
Thinking Time 7																							
Iteration 8																							
Final iteration																							
Verify final state																							
Week 2 Latest Modification Date and Range																							
Week 3 Decision Date and Range																							

6.3.1 Day 1 (Iteration 1)

Iteration 1 gets us up to speed on how things are doing with the nominal launch configuration, and gets us some data for the first set of adjustments. Since it's the first hard look after we get on orbit, we throw the kitchen sink at it.

6.3.1.1 Realtime Uplink (Section 6.2)

It is possible that, based on ACS-R FT information or from testing before SMOV, we know we need to make a change before the start of the Optimization Campaign. A realtime uplink window should be established to allow for this possibility. We do not expect this uplink to be used.

6.3.1.2 Oscilloscope Mode Readout Of Internal Signals (Section 6.1.4)

Dump timing relationship of external signals to ASIC references.

Analysis responsibility: ACS-R Hardware Team (Teledyne lead)

6.3.1.3 Starting Performance (Section 6.1.3)

Perform a Performance Summary data run to get the starting performance levels.

Analysis responsibility: STScl

6.3.1.4 Check Preamp Settling (Section 5.1)

Take a set of preamp settling data around the nominal value of the Reset Gate clock rails. It will take a day to determine whether the nominal is OK, and if not, what adjustment is desired and what realtime command needs to be generated.

6.3.1.5 Check Clock Feedthrough (Section 5.2)

Perform the clock feedthrough tests. It will take at least one day to determine any adjustments needed for the timing patterns and to generate the realtime commands to implement the change.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.1.6 Check Biases And Clock Rails (Section 5.3)

Find optimum bias and clock rail voltages using the default timings. These data will probably take ~2 days to analyze and to generate the realtime commands required to set the desired voltages.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.1.7 Science Data Transmission Timing (Section 5.6)

Map readout noise for variations of timing parameters around the initial values.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.2 Day 2

Thinking ...

6.3.3 Day 3

Thinking ...

6.3.4 Day 4

Thinking ...

6.3.5 Day 5 (Iteration 2)

We assume at this point that we have the optimal settings from the Preamp Settling measurements for Reset Gate as well as the first optimization for the Science Data Transmission Timing. This iteration focuses on the Clock Feedthrough.

Decide if last minute changes are needed to the week 2 SMS (if everything is perfect we can just terminate the Optimization Campaign).

6.3.5.1 Realtime Uplink (Section 6.2)

Before any of the subsequent tests, the realtime parameter uplinks occur from the Day 1 tests.

Responsibility: HST Ops

6.3.5.2 Oscilloscope Mode Readout Of Internal Signals (Section 6.1.4)

Dump timing relationship of external signals to ASIC references.

Analysis responsibility: ACS-R Hardware Team (Teledyne lead)

6.3.5.3 Performance Summary (Section 6.1.3)

Perform a Performance Summary data run to get the starting performance levels.

Analysis responsibility: STScl

6.3.5.4 Check Clock Feedthrough (Section 5.2)

Perform the clock feedthrough tests.

Note that the next realtime commanding opportunity will need to reset any rails that are modified by this test back to the optimal values determined by previous on-orbit testing. These optimal values get overwritten when we run this test, and the SMS does not know what to set these back to.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.6 Day 6

Thinking ...

6.3.7 Day 7

Thinking ...

6.3.8 Day 8 (Iteration 3)

We assume at this point that we have optimized the Preamp Settling, Clock Feedthrough, and Science Data Transmission Timing. The last remaining topic is the Clock and Bias Voltages.

6.3.8.1 Realtime Uplink (Section 6.2)

Before any of the subsequent tests, the realtime parameter uplinks occur from the Day 5 tests.

Responsibility: HST Ops

6.3.8.2 Oscilloscope Mode Readout Of Internal Signals (Section 6.1.4)

Dump timing relationship of external signals to ASIC references.

Analysis responsibility: ACS-R Hardware Team (Teledyne lead)

6.3.8.3 Performance Summary (Section 6.1.3)

Evaluate the effects of the previous changes.

Analysis responsibility: STScl

6.3.8.4 Check Biases And Clock Rails (Section 5.3)

Find optimum bias and clock rail voltages using the new set of configuration parameters.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.9 Day 9

Thinking ...

6.3.10 Day 10

Thinking ...

6.3.11 Day 11

Thinking ...

6.3.12 Day 12 (Iteration 4)

At this point, we recheck the Clock Feedthrough and fine-tune the timing pattern tables if necessary.

Decide if changes are needed to the week 3 SMS, including truncating the Optimization Campaign. If the week 3 SMS is to continue the optimization effort, *the SMS sequences should be modified* to use the current default values that are being uploaded in realtime as the new optimal values.

6.3.12.1 Realtime Uplink (Section 6.2)

Before any of the subsequent tests, the realtime parameter uplinks occur from the Day 8 tests.

Responsibility: HST Ops

6.3.12.2 Oscilloscope Mode Readout Of Internal Signals (Section 6.1.4)

Dump timing relationship of external signals to ASIC references.

Analysis responsibility: ACS-R Hardware Team (Teledyne lead)

6.3.12.3 Performance Summary (Section 6.1.3)

Evaluate the effects of the previous changes.

Analysis responsibility: STScl

6.3.12.4 Check Clock Feedthrough (Section 5.2)

Perform the clock feedthrough tests.

Note that the next realtime commanding opportunity will need to reset any rails that are modified by this test back to the optimal values determined by previous testing. These optimal values get overwritten when we run this test.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.12.5 Science Data Transmission Timing (Section 5.6)

Map readout noise for variations of timing parameters around the initial values.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

Thinking ... **6.3.13 Day 13**

Thinking ... **6.3.14 Day 14**

Thinking ... **6.3.15 Day 15**

6.3.16 Day 16 (Iteration 5)

This is potentially the last day for uplinking and testing if we decided to terminate the optimization at 2 weeks (back on Day 12).

If we are stopping, then we gather this data to verify and document the final state.

If we are not stopping, we continue with the week 3 SMS.

6.3.16.1 Realtime Uplink

This is the (potentially) final realtime uplink adjustment.

Responsibility: HST Ops

6.3.16.2 Oscilloscope Mode Readout Of Internal Signals (Section 6.1.4)

Dump timing relationship of external signals to ASIC references.

Analysis responsibility: ACS-R Hardware Team (Teledyne lead)

6.3.16.3 Performance Summary (Section 6.1.3)

Perform a Performance Summary data run to get the (potentially) ending performance levels.

Analysis responsibility: STScl

6.3.16.4 Check Clock Feedthrough (Section 5.2)

Perform the clock feedthrough tests.

Note that the next realtime commanding opportunity will need to reset any rails that are modified by this test back to the optimal values determined by previous testing. These optimal values get overwritten when we run this test.

6.3.17 Day 17 (Iteration 6)

This is the start of the week 3 SMS. *The tests described from now on should include the newly-determined optimal values of parameters that were known on Day 12.* These are the parameters that specify “nominal” in the tests that make variations around the nominal values.

Since we are starting with a new set of defaults, we repeat the tests for the first iteration.

6.3.17.1 Realtime Uplink

A realtime uplink is not likely to be required because that was completed on Day 16. Still, one should be scheduled in case something needs correction, or a change that was too late for Day 16 is available now.

Responsibility: HST Ops

6.3.17.2 Check Preamp Settling (Section 5.1)

Take a set of preamp settling data around the nominal value of the Reset Gate clock rails.

6.3.17.3 Check Clock Feedthrough (Section 5.2)

Perform the clock feedthrough tests.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.17.4 Check Biases And Clock Rails (Section 5.3)

Find optimum bias and clock rail voltages using the default timings.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.17.5 Science Data Transmission Timing (Section 5.6)

Map readout noise for variations of timing parameters around the initial values.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.18 Day 18

Thinking ...

6.3.19 Day 19

Thinking ...

6.3.20 Day 20 (Iteration 7)

It's a toss-up which test to perform for this iteration since that depends on the problem we are running up against. This placeholder runs the first iteration tests again.

6.3.20.1 Realtime Uplink

Before any of the subsequent tests, the realtime parameter uplinks occur from the Day 17 tests.

Responsibility: HST Ops

6.3.20.2 Check Preamp Settling (Section 5.1)

Take a set of preamp settling data around the nominal value of the Reset Gate clock rails.

6.3.20.3 Check Clock Feedthrough (Section 5.2)

Perform the clock feedthrough tests.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.20.4 Check Biases And Clock Rails (Section 5.3)

Find optimum bias and clock rail voltages using the default timings.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.20.5 Science Data Transmission Timing (Section 5.6)

Map readout noise for variations of timing parameters around the initial values.

Analysis responsibility: ACS-R Hardware Team (DCL lead)

6.3.21 Day 21

Thinking ...

6.3.22 Day 22

Thinking ...

6.3.23 Day 23 (Iteration 8)

This is the last day of the planned Optimization Campaign.

6.3.23.1 Realtime Uplink

This is the final realtime uplink adjustment.

Responsibility: HST Ops

6.3.23.2 Oscilloscope Mode Readout Of Internal Signals (Section 6.1.4)

Dump timing relationship of external signals to ASIC references.

Analysis responsibility: ACS-R Hardware Team (Teledyne lead)

6.3.23.3 Performance Summary (Section 6.1.3)

Perform a Performance Summary data run to get the ending performance levels.

Analysis responsibility: STScl

6.3.24 Transition to Normal SMOV Activities

After the Optimization Campaign, the ACS-R will transition to normal SMOV operations that perform the detailed science calibrations. This is nominally the same plan that was used for the original ACS deployment SMOV.

6.4 Recordkeeping and Processes

A significant amount of data will be taken during the relatively short Optimization Campaign.

A master procedure will be used to control the activities during the Optimization Campaign.

A data management plan needs to be generated to make sure the data are appropriately organized to support rapid decisions.

In particular:

1. All data take shall be keyed to which steps in the master procedure it came from.
2. All data taken shall be archived and readily retrievable.
3. All requested adjustments with rationale shall be noted by systems, and shall have supporting documentation and analyses attached and keyed to the master procedure.
4. Anomalies observed shall be tracked down using normal systems approaches (fishbone diagram, etc.).
5. "Outstanding/pending questions" list shall be maintained by systems.

7 Data Analysis Concept And Tools

7.1 Data Availability

Data is assumed to be available shortly after execution. This is anticipated to be within 12 (TBR) hours. It is understood that the EPER frames are the most data volume intensive, and could arrive in pieces that have to be reassembled.

A plan will be put in place to exercise the data transfer process well before launch. We require this data on short notice because the cadence of the adjustments needs to be relatively fast.

7.2 Data Formats

The DCL and Teledyne analysis teams will need to be able to ingest SDI and POD file formats.

7.3 Analysis Mode

To support the rapid turnaround, especially for the events, automated analysis will be required. Appropriate software will be developed to support the analyses specified in this plan.

7.4 Analysis Tools

The following specific analysis tools will be required to perform the CEB-R optimization. This table summarizes the scope and the responsible parties. Please refer to the text for more detailed descriptions. (Specific names are provided for tasks that are already completed or in progress.)

Tool	Responsible Party
Pre-Failure Interesting Pixel Identification	Don Lindler
Basic Display Of Oscilloscope Mode Data	Jing Chen
Panel Display of Oscilloscope Mode Data	Jing Chen
Overlay Display of Oscilloscope Mode Data	Jing Chen
Calculated Signal Level From Oscilloscope Mode Data	Jing Chen
Preamp Settling Analysis	DCL
Clock Feedthrough Analysis	DCL
Bias and Clock Voltage Analysis	DCL
Parallel Clock Setting	STScI
Science Data Transmission Timing	DCL
Performance Summary	STScI
Oscilloscope Mode Readout Of Internal Signals	Jing Chen

7.4.1 Pre-Failure Interesting Pixels

The Oscilloscope Mode configuration tables require a set of 40 positions that will be sampled for all four quadrants of the CCD. To determine these positions, we look at the pre-failure bias frames and attempt to select a set that contains both “normal”, and “interesting” pixels to look at. These positions will be encoded into the final flight build

of the Flight Assembly Code for the ASIC. They can be adjusted on-orbit if necessary by overwriting a table that is initialized when the ASIC starts up.

7.4.2 Basic Display Of Oscilloscope Mode Data

When the Oscilloscope Mode data reaches the ground, it needs to be made available as a FITS image or some other comparable format. The ACS-R team will need special software to interpret these images and provide plots of the Oscilloscope Mode data that the file contains. Note that each “pixel” refers to a capture, which is actually several pixels long. The plots should include the entire capture, or at least a way of viewing the entire capture, with pixel boundaries clearly marked.

When plotting the traces (as a function of time), it would be helpful to have some bars drawn at the times where the major internal clocks are changing state. For instance, Summing Well and Reset Gate, and perhaps also the last Serial Clock edge. This information can be retrieved from the configuration information. A selection box can be used to allow the user to pick the annotation desired.

Each plot should clearly label the pixel number that the data came from. This can be in normal coordinates used for the full CCD. It should also show the index number and the pixel coordinates specified by the configuration registers (these pixel coordinates refer to the coordinates within a quadrant).

7.4.3 Panel Display Of Oscilloscope Mode Data

It will be useful to have a display mode that allows an array of little Oscilloscope Mode plots on the page. Each of these would have a trace and some of the information described in Section 7.4.2.

This display mode should have the ability to take a list of pixels that will be processed in this manner so that only selected pixels are plotted.

7.4.4 Overlay Display Of Oscilloscope Mode Data

It will be useful to have a display mode that allows overplotting of multiple pixels that are displayed in the manner of Section 7.4.2.

This display mode should have the ability to take a list of pixels that will be processed in this manner so that only selected pixels are plotted.

7.4.5 Calculated Signal Level From Oscilloscope Mode Data

Based on the configuration register timing information and the Oscilloscope Mode data, it is possible to reconstruct what the video electronics would return as a signal value for a pixel. This will have higher noise, but in many cases is sufficient. There should be the option of including these reconstructed video signals into the display products.

7.4.6 Preamp Settling Analysis (Section 5.1)

Tools/scripts will be prepared to support these analyses.

7.4.7 Clock Feedthrough Analysis (Section 5.2)

Tools/scripts will be prepared to support these analyses.

7.4.8 Bias And Clock Voltage Analysis (Section 5.3)

Tools/scripts will be prepared to support these analyses.

7.4.9 Parallel Clock Settling (Section 5.4)

Tools/scripts will be prepared to support these analyses. The current approach is to compare newly acquired EPER frame CTE results with the extrapolated CTE expected based on the additional radiation exposure since the ACS failure.

7.4.10 Science Data Transmission Timing (Section 5.6)

The test will generate a set of data that spans some reasonable settings of the Science Data Control Register, centered around the ground test optimum value. A tool will be prepared that takes these data and plots them up to show the noise dependence on the settings.

Only one CCD output will be used (Channel B), so there will only be one such plot.

This plot will show the increase in noise as a particular parameter is varied, with the other parameters set to the minimum-noise values. Each plot will have one subsection for each of the three parameters in this register.

7.4.11 Performance Summary (Section 6.1.3)

This can probably be accommodated using standard processing and tools at STScI. It is particularly important that we be able to assess inter and intra-CCD crosstalk using some dark frames and the hot pixels in the CCDs.

7.4.12 Oscilloscope Mode Readout Of Internal Signals (Section 6.1.4)

Tools/scripts will be prepared to support these analyses. A report will be generated that confirms that the observed clocks are what we expect based on the timing patterns being executed.

7.5 Development Tools

Test scripts that simulate the data taken during the planned operations will be used to verify that the ACS-R hardware performs as expected in the lab (with the CEB-R Test Set). These scripts implement the same tests as the on-orbit cases, and should be used to generate the data required for verifying the analysis processes and procedures.

8 Operations, Training, and Staffing

A procedure will be generated that details the specific activities required to execute this plan.

Simulations of the activities addressed by this plan will be conducted to help ensure smooth execution. This will include:

1. Data storage and retrieval.
2. Data transfer operations that exercise the data paths that will be needed.
3. Communication paths, as required by the procedure.
4. Complete analysis results using simulated data.
5. Lab hardware emulation of on-orbit results, including operation of the ACS5 detector enclosure with the Offner projection system at the DCL.

Anticipated key participants during the SMOV CEB-R Optimization Campaign are:

Kevin Boyce (GSFC)
Kathleen Mil (GSFC)
Erin Wilson (GSFC)
Don Lindler (GSFC)
Augustyn Waczynski (DCL)
Markus Loose (TIS)
Raphael Ricardo (TIS, remote)
Jing Chen (TIS)
Marco Sirianni (STScI) et al.

These team members will participate in developing the planned activities, in implementing the tools required, and in simulating the optimization process.

END