NICMOS Dark Current Anomaly: Test Results

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ABSTRACT

We report on the results of a laboratory test program to investigate the nature of the NICMOS dark current anomaly. The test was designed to investigate one proposed mechanism of signal electrons - excited into the conduction band by infrared photons - being stored at low temperatures in charge traps throughout the detector material and released during warmup. The test did not reproduce the bump, and the proposed scenario could not be confirmed. The nature of the anomaly thus remains unexplained. We discuss this result with regard to possible alternative explanations and options for testing them.

1. Introduction

The NICMOS dark current anomaly (a.k.a. "the bump") detected during the instrument warm-up in January 1999 was extensively discussed in ISR NICMOS-99-001. In an attempt to understand this anomalous behavior, the NICMOS group consulted with both detector manufacturers as well as theorists. During these consultations, the theory developed that charge - excited by infrared photons - was trapped in the detector material at low temperatures, and released as the detector heated up. To explore this hypothesis, a test plan was set up in collaboration with the NICMOS Investigation Definition Team (IDT) at the University of Arizona, which is described in detail in ISR NICMOS-99-009. Briefly, the procedure was to measure the dark current as a function of temperature for a NICMOS flight spare detector - from the same manufacturing lot as the flight detectors - before and after illumination in the cold state. The commanded temperature sequence for the test was intended to replicate as closely as possible the measured warmup profile of NICMOS on orbit. In this ISR, we describe in Sec. 2 the laboratory setup, the test sequence, and some minor hardware problems that were encountered over the course of the test. In Sec. 3 we

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summarize the data quality and analysis method. The results of the analysis are presented in Sec. 4, which demonstrate that no anomalous dark current increase above the levels expected at elevated temperatures was observed. We also discuss the results in the context of possible alternative explanations for the bump, and evaluates options for future tests. We conclude in Section 5 with a discussion of the implications for NICMOS science operations in Cycle 10.

2. Test Equipment, Test Sequence, and Hardware Problems

Equipment

- ***Detector:*** The NICMOS3 flight spare array chosen from the UofA inventory has the device number 79T0012. It is similar in most characteristics to the on-orbit flight detectors. The device is known to have intrinsically low levels of dark current - significantly lower than the ~ 0.35 e^-/s systematic background which was maintained during the warm-up testing with our dewar and readout electronics as configured. The device was originally characterized in 1994 during the screening and selection process for choosing the flight arrays for HST. Although a high quality unit, it was relegated to "flight spare" status on the basis of its long reset anomaly time constant (see Sec. 3) and somewhat lower DQE. For this test we did not perform a re-characterization of the device, as its behavior remained essentially stable since its initial screening. In those tests, which were performed by Rockwell Int., a device conversion gain of 11.73 e^-/DN was measured.
- ***Test Dewar and Thermal Control:*** All testing was performed with device 79T0012 mounted in a "light" dewar (i.e., one in which the detector can be stimulated by an external light source through a cold-shuttered optical window) taken from the NICMOS Project inventory at Steward Observatory. The dewar, model number HDL-8, was procured from IR Labs, and designed for liquid He cooling. A separate LN_2 cooled shield acts as a thermal buffer to keep the ~300 K outer case from inducing a large thermal load on the He cooled shield. When so configured, at a stage temperature of 63 K the hold time for this unit is approximately 12 hours. An internal cold shutter which blanks off the external optical path is maintained at 4 K to allow dark current measurements to be made. Beyond the window are two filter wheels which can be externally commanded and rotated for Q.E. testing and optical stimulation at selected wavelengths.
- ***Filters:*** Four filters were chosen to flood illuminate the detector at selected wavelengths. The filter set employed had central wavelengths of 0.8, 1.2, 1.8, and 2.4 µm, and all had bandwidths (FWHM cut-on/cut-off) of 0.1 microns. The filters were manufactured by Oriel and are of similar pedigree to the medium bandwidth NICMOS flight filters. The filters were mounted in the dewar's filter wheel and cooled by the LN_2 shield to 77K.

- ***Thermal background:*** Low thermal backgrounds were maintained through the entire duration of the test. The LHe shield never exceeded 10 K. The inside of the shields is coated with IR absorbing paint. The dewar and array were cooled to 63 K and held at this temperature for five days to allow for complete equilibration and stabilization before the start of the bump test.
- ***Readout Electronics:*** The readout electronics employed for the bump test were designed by San Diego State University (SDSU) with video boards modified by IR Labs to work with IR detectors. Because of the extensive use of SDSU controllers at Steward Observatory, primarily on CCD cameras, we elected to use the same setup in this test. Standard observing software using the IRAF Control Environment (ICE) was modified to allow a NICMOS array to be clocked in a flight-like manner with timing and voltages reproducing STEP64, NSAMP=26 readout sampling.
- ***Heater Control:*** The heater control unit used for the test was a Lakeshore Model 330 Autotuning Temperature Controller. A Linux PC computer was connected to the serial command and data lines of the controller used as a continuous data logger and to set and change the temperature set-points and warm-up rates. A web based interface provided was developed for test personnel to monitor and/or control the test either in the detector lab or remotely.
- ***Light source:*** The external stimulus was a Gilway 8010 lamp, the same type used in the NICMOS internal flat field illuminator module. This lamp was retained from the original lot used in lamp mortality and life-cycle testing which was done pre-flight at Steward Observatory. For the tests described here, the lamp was operated at 4.52 V and 750 mA. Under those conditions, the blackbody temperature of the lamp was 2420 K. The lamp was mounted on a stand and aimed at a white diffuser card which presented a large viewing angle to the optical entrance port of the downward-looking dewar. At long wavelengths the diffuse thermal background of the room contributed significantly to the total illumination.

Test procedure

The test sequence had the following four phases:

1. ***Pre-flood phase***: The detector was cooled to 63.4 K and allowed to thermally stabilize. A set of baseline dark exposures were taken at this temperature. The detector was then heated up to 88 K following a commanded temperature profile which consisted of 14 linear ramp segments (see Appendix A) chosen to closely follow the observed profile of NICMOS after the cryogen depletion (Fig. 1). During the entire duration of the warmup (about 5 days), STEP64 MULTIACCUM exposures were taken, with NSAMP=25 each with a total exposure time of 1088 s. The pre-flood phase was intended to provide a baseline measurement of the detector dark current as a function of temperature **without any prior illumination**.
2. ***Flooding***: The detector was cooled back to 63.4 K and another set of baseline darks was obtained at this temperature as a consistency check with the previous data. The detector was then illuminated in four passbands over its entire sensitivity range. Table 1 contains the details of the flooding. The DQE in each of the bands at

the the flooding temperature of 63 K was estimated from the pre-launch qualification data which were obtained at 58 K. The basic consideration that determined the flooding levels was to provide sufficient signal to produce the total amount of charge released throughout the course of the bump, i.e. 8×10^5 e^-/pixel. Since the probability for a given electron to be trapped is unknown, a total flood level about 1000 times higher was considered a good compromise between the duration of the flooding and the probability of filling the putative traps. As can be seen from Table 1, the accumulated signal during the flooding over the four passbands was 1.6×10^9 e^-/pixel.

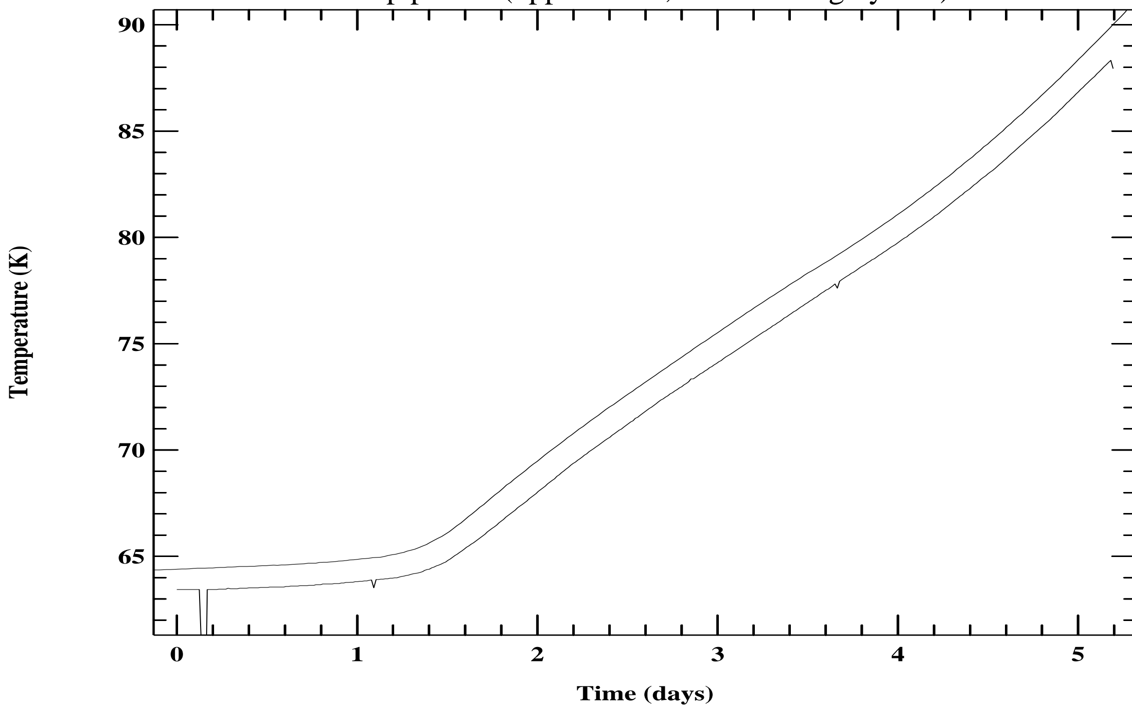
3. ***Post-flood phase***: After the flooding at 63.4 K, the warmup profile described in Step 1 was identically repeated. If the proposed scenario of trapped charge had been correct, this sequence should have reproduced the on-orbit dark current profile, including the bump.

4. ***Dwell test:*** The detector was again cooled to 63.4 K. After thermal stabilization, baseline darks were again obtained to provide comparison to the previous measurements. The detector was then warmed up following the temperature profile shown in Figure 2. The temperature was rapidly raised between a series of dwell points (63.4, 70, 77, 83, and 88 K), allowing the detector to equilibriate at each point. Once thermal equilibrium was achieved, dark exposures were taken in the same way as described above. The reasoning behind this sequence was to check for thermal lags of the chip temperature which might occur during the ramp tests because of imperfect coupling between the chip and the detector stage.

Table 1. Summary of illumination levels per detector pixel. The rows give i) the central wavelength of the filter, ii) the FWHM of the filter, iii) estimated median DQE at 63 K, iv) the signal per pixel - averaged over the array - during the flooding, v) the duration of the flooding, vi) the total signal per pixel collected over the flooding.

	Filter 1	**Filter 2**	**Filter 3**	**Filter 4**
λ_c [μm]	0.8	1.2	1.8	2.4
$\Delta\lambda$ [μm]	0.1	0.1	0.1	0.1
DQE [%]	15	40	60	80
I [ADU s^{-1} $pixel^{-1}$]	3409	6383	10936	9189
Δt [min]	54	74	66	108
Σ [$10^8 e^-$ /$pixel^{-1}$]	1.30	3.33	5.08	6.99

Figure 1: Detector stage temperature profile for ramp tests (lower curve) in comparison to the measured on-orbit warmup profile (upper curve, after shifting by 1 K).

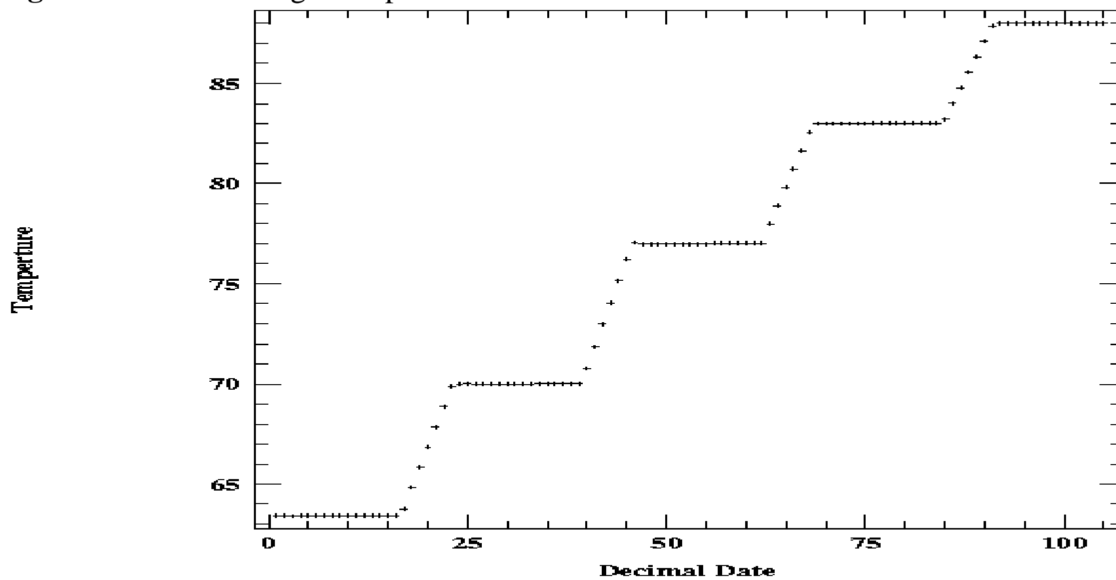


Hardware Anomalies

During the course of the test sequence, minor hardware problems were encountered in both the heater control and the readout electronics. The problems caused the loss of some data sets, but did not compromise the validity of the test as a whole:

- **Heater Dropouts:** For as of yet unexplained reasons, the heater control electronic had several glitches over the course of the tests. Basically, at apparently random times throughout the warmup profile, the controller would turn off the heater. A “watchdog” program was written and used to detect these instances in the shortest possible amount of time. Immediately after detection of a heater dropout, the program would reset the heater control, so that the originally programmed profile was recovered in less than 2 minutes. Nevertheless, the few short temperature drops caused by these instances are easily seen in Figure 1. The dark current exposures taken during these dropouts show anomalously high bias variations due to the steep temperature gradient, and were discarded from the analysis. For each dropout occurrence - a total of five over the whole test sequence - only one exposure was affected.
- **Electronics failure:** During the second, post-flooding warmup ramp, an anomaly occurred in the detector readout electronics. Apparently, the Analog-to-Digital Converter (ADC) was using out-of-range voltages for a period of about 4 hrs, until the electronics was reset and normal operations resumed. The temperature profile was unaffected by this anomaly, however, data taken during this period (14 MULTI-ACCUM sets between 74 and 76 K) were corrupted and unusable.

Figure 2: Detector Stage Temperature Profile for Dwell Test



3. Data Quality and Reduction Procedures

Odd/Even Bias Fluctuations

The readout electronics used for the tests imprints bias variations on the dark current exposures which are high/low in odd/even columns. The pattern of vertical stripes is, however, very repeatable and noiseless. It subtracts out completely when subtracting two reads of a MULTIACCUM sequence (Fig.3), and therefore does not degrade the noise properties of the system.

Residual noise sources and error estimate

While the subtraction of two reads eliminates the odd/even pattern in the images, it reveals a residual noise component caused by the 60 Hz power supply frequency as shown in Fig. 3. Due to this time-variable noise pattern, the signal for individual pixels varies significantly between frames, and the derived dark current for single pixels is therefore not reliable. However, averaging over a large region on the chip reduces the impact of the pattern position. In order to assess the impact of the 60 Hz noise, we have computed the average signal in box [30:226,30:226] in the difference image of all possible read pairs (excluding reads affected by the reset anomaly, see below) of a given MULTIACCUM sequence. The RMS variation of the derived values then yields an error estimate for the dark currents. Combining frames taken at the same temperature allows to improve the statistics further. Fig. 4 shows the histogram for all MULTIACCUMs taken at temperatures between 63.4 and 63.8 K, including both pre- and post-flood data. The mean of the distribution is 0.38 e^-/s with a standard deviation of 0.06 e^-/s. We therefore estimate the error in the dark current measurements to be about 15%.

Figure 3: Odd/Even Fluctuating Bias (left) and 60 Hz noise (right). In each image, one detector quadrant is shown. The left image is from a single read of a MULTIACCUM sequence, while the right image was obtained by subtracting two reads. The subtraction of two frames eliminates the effects of the stable odd/even pattern, and makes the 60 Hz component visible (the grayscale stretch of the right image has been optimized to show the residual structure).

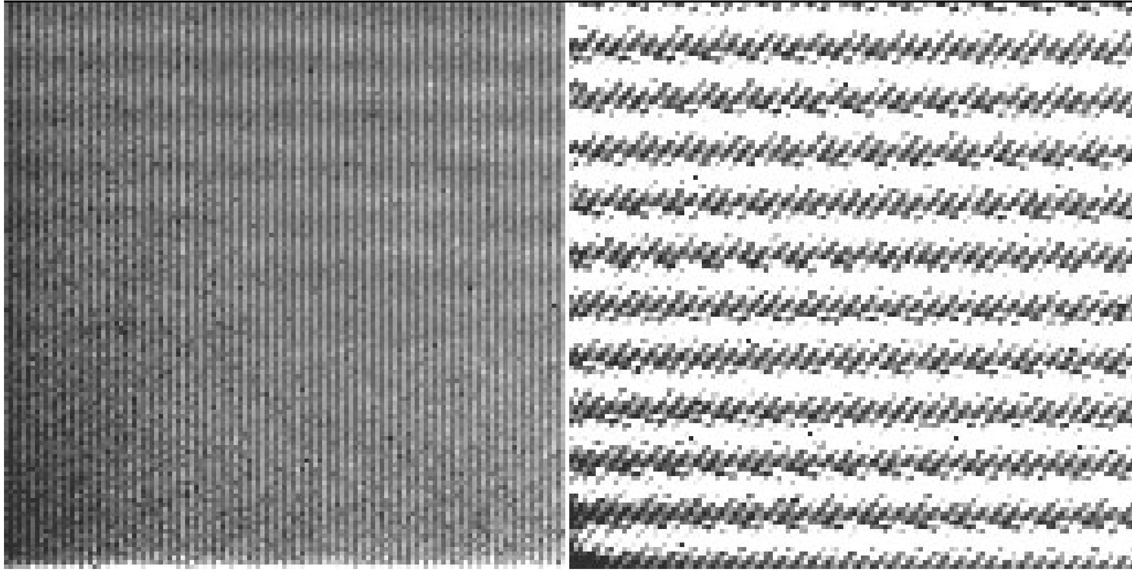
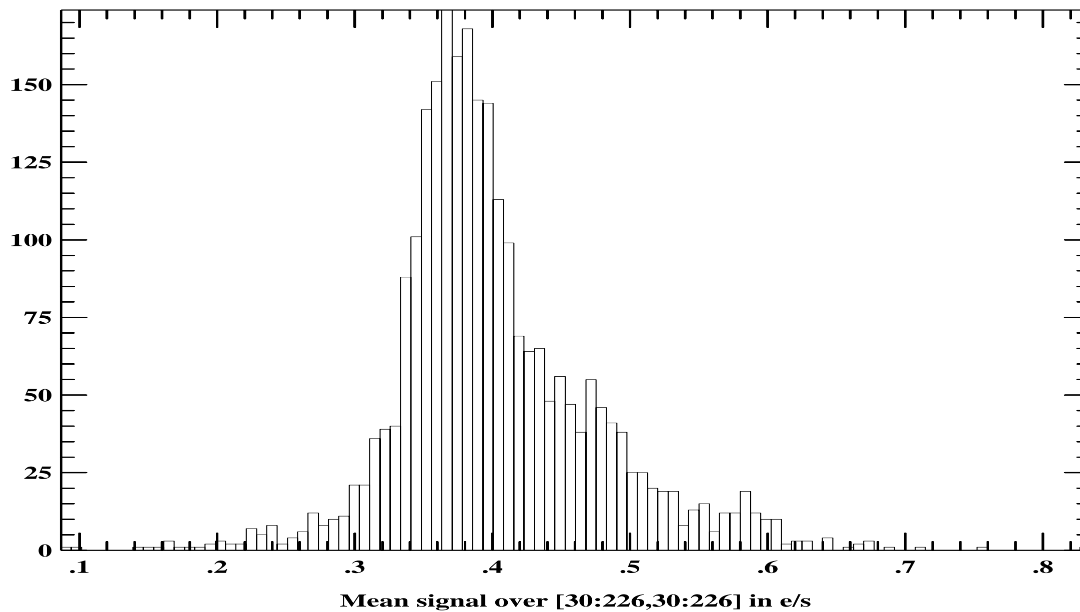


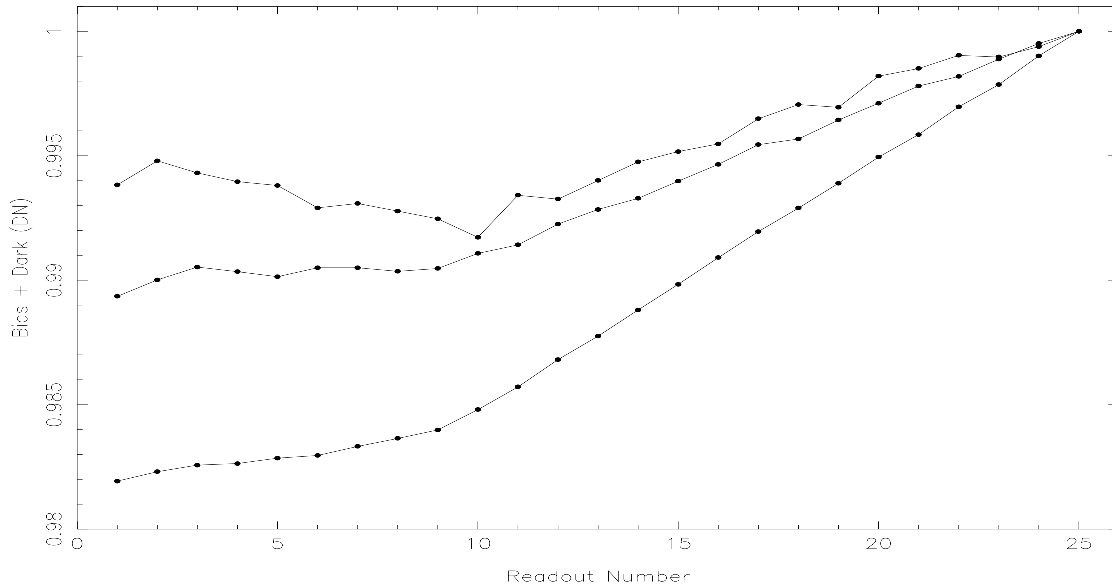
Figure 4: Histogram of mean signal for all possible read pairs of MULTIACCUMs taken between 63.4 and 63.8 K.



Reset anomaly (the “hook - phenomenon”)

Many NICMOS3 detectors are known to exhibit a slow bias recovery after a reset pulse. The consequence of this behavior is that the detector needs a substantial time before it enters the linear regime. The behavior is demonstrated in Fig. 5 which shows the behavior of a dark exposure sequence (NSAMP=25 STEP64 MULTIACCUM) at three different temperatures. Note that the linear regime does not begin before read 12. To be conservative, we used the difference between reads 25 and 14 to determine the accumulated dark current. The effective integration time between these two reads is 704 s.

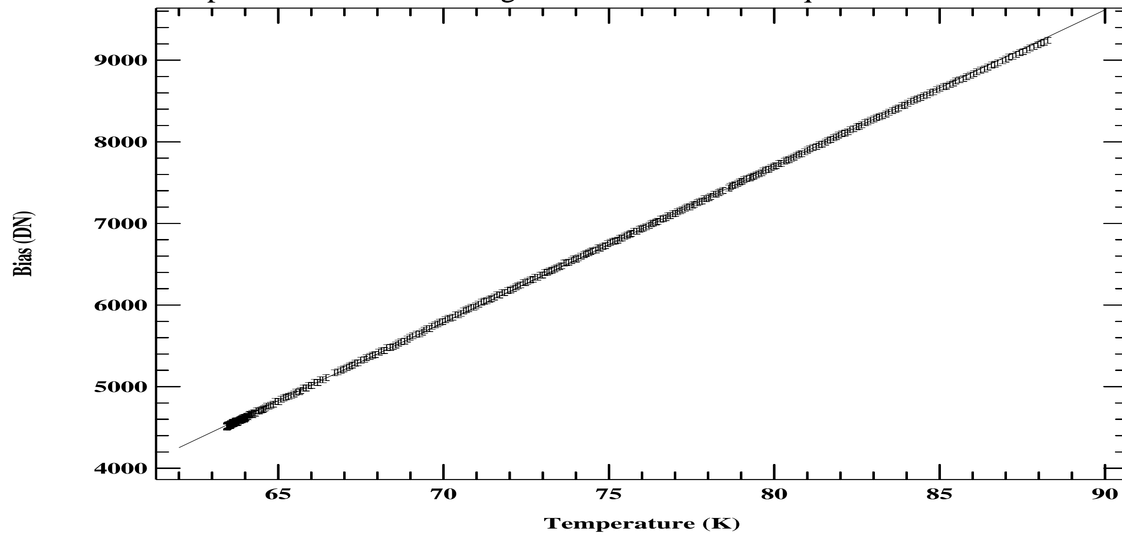
Figure 5: Reset Anomaly. Shown are the average signals along a MULTIACCUM sequence at three different temperatures, normalized to the signal in read 25.



Temperature dependence of the detector bias

The detector bias is known to be extremely sensitive to temperature variations. NICMOS3 detectors therefore make excellent thermometers. Fig. 6 shows the mean signal in the 0th read for all MULTIACCUM sequences obtained during the first (“pre-flood”) series as a function of mounting stage temperature. The best fit slope for the data in Fig. 6 is 191.6 DN/K, it was used to initially correct the measured dark current for the temperature increase throughout an exposure (see below). However, it is important to note that the stage temperature is not necessarily an accurate measure of the chip temperature during the ramp tests because of imperfect mechanical coupling (see discussion in Sec. 4). The slope derived from Fig. 6 is likely to be an underestimate of the true value because the detector is lagging behind the stage during the temperature ramps.

Figure 6: Bias variations with temperature. The linear behavior allows an accurate correction for the temperature increase during a MULTIACCUM sequence.



Reduction Procedure

The basic data reduction procedure was as follows:

- Take the difference between reads 25 and 14 of each MULTIACCUM sequence. This eliminates the odd/even pattern, possible bias variations, and avoids using reads which are affected by the reset anomaly described above.
- Determine the mean dark current over a large region on the chip. We chose region [30:226,30:226] in order to avoid the elevated signal in the corners of the array due to amplifier glow.
- Correct the derived dark current in DN/s for the bias change caused by the temperature increase between reads 25 and 14. Since the detector temperature changed slightly, but noticeable during the course of the 704s integration time between the two reads, the detector bias - which is very sensitive to temperature changes, see Fig. 6 - was different for the two reads. The measured dark current must be corrected for this effect. The temperature difference ΔT between reads 14 and 25 for each MULTIACCUM sequence was determined from the temperature sensor data which were sampled every 30 s. Assuming that the sensor data are an accurate representation for the chip temperature, the bias change follows directly from ΔT. However, as mentioned before, this might not be the case, and an additional empirical correction factor had to be applied which will be discussed further in Sec. 4.
- Convert the corrected dark current signal from DN to e^-/s through multiplication by the electronic gain, and division by the integration time (704 s). For the detector used in these tests, a gain of 11.73 e-/DN was adopted from its initial screening tests.

4. Results and Discussion

As mentioned above, the dwell test was designed to check for possible discrepancies between the stage sensor data and the true chip temperature. Since during these tests the detector was held at a stable temperature, no ΔT-correction is necessary, and the stage temperature is an accurate measure of the chip temperature. However, for the ramp test, there is likely to be a temperature difference between the stage and the detector. This means that the applied bias correction between the two reads as derived from Fig. 6 is not correct. The measured slope is underestimating the true bias variation with temperature, because the detector is in fact somewhat colder than the stage. This is plausible and somewhat expected because the mechanical coupling between the chip and its mounting stage is never perfect.

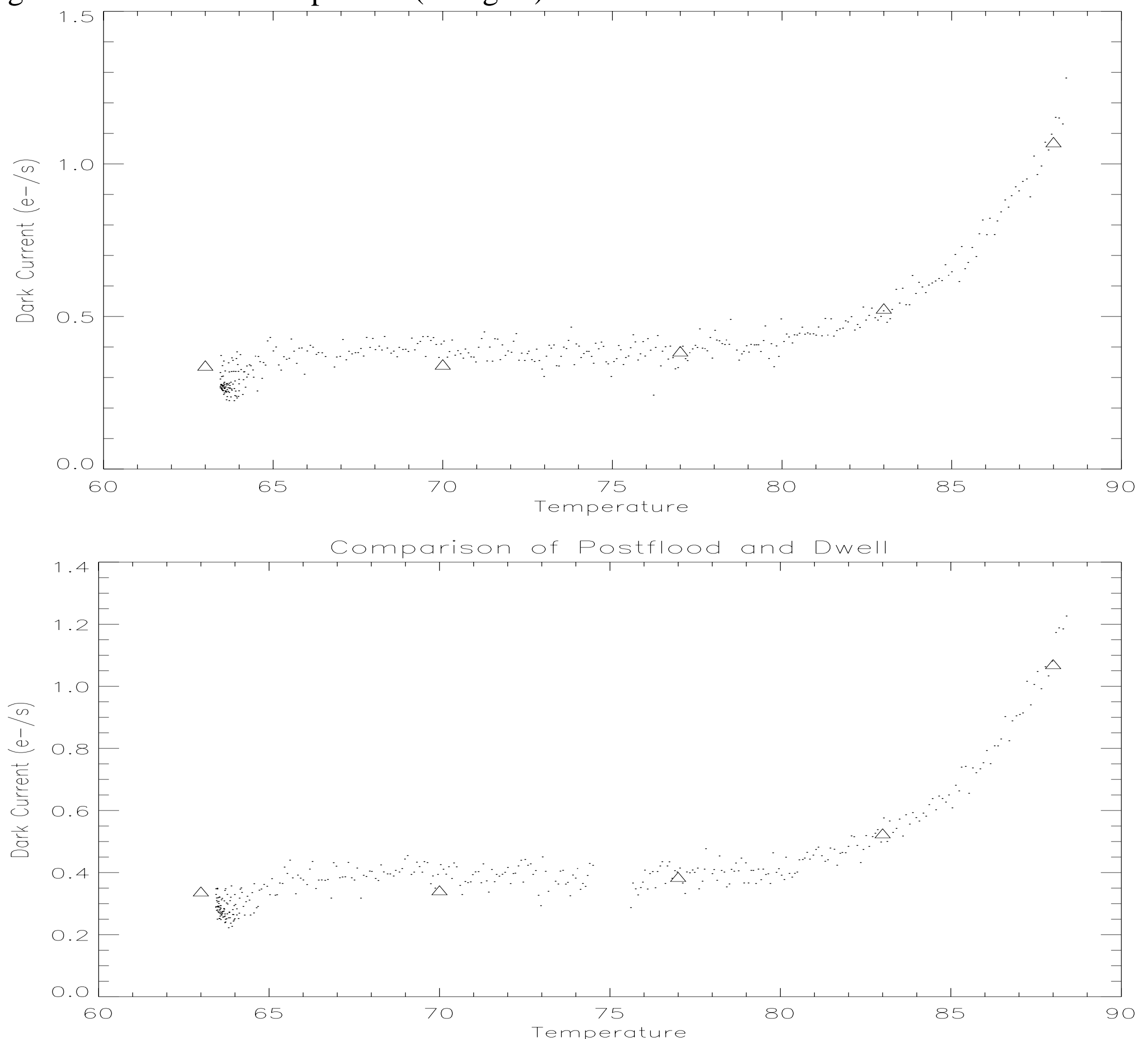
We correct for this thermal lag by multiplying the dark current values derived from the ramp test by a correction factor such that they agree with the dwell test results. The required correction amounted to roughly a 40% reduction. The resulting curve of the dark current as a function of temperature for both the pre- and post-flood measurements are plotted in Fig.7 which also contains the measurements from the dwell points (asterisks). Both curves are completely consistent with each other, and certainly show no evidence for an anomalous dark current behavior. The bump observed during the on-orbit warmup had a peak signal of about 2.7 e^-/s at 82 K, so it would be clearly visible in Fig. 7.

The relatively flat dark current level of ~0.35 e^-/s in the temperature range between 64 and 75 K indicates that the measurements in this regime are not reflecting the true intrinsic dark current, but rather are limited by the thermal background inside the dewar.

Because no bump was found in these tests, the scenario described in ISR NICMOS-99-009 could not be confirmed. In that report, it was suggested that a population of charge traps located at the CdTe-HgCdTe interface and produced during the manufacturing process is responsible for the dark current bump. Since the detectors used for the tests described here are from the same manufacturing batch, it follows that either the levels of infrared illumination used during these tests were insufficient to populate a large number of traps, or that any existing charge traps are specific to the on-orbit detectors - possibly caused by exposure to cosmic radiation. The explanation of insufficient light levels seems rather unlikely, based on the complete absence of any dark current elevation despite the relatively high illumination dosage.

In order to test the second hypothesis that cosmic rays are responsible for producing the charge traps, the program described here should be repeated with a detector chip that has been exposed to high-energy proton radiation. Possible low-cost opportunities for such tests exist in conjunction with the radiation test program of the IR-detectors for WFC3.

Figure 7: Dark current vs temperature derived after the described data reduction. Top: pre-flood, bottom: post-flood data. The gap around 75 K in the post-flood data is due to the electronics failure mentioned in Sec. 3. Both panels show the dark current measured during the dwell test for comparison (triangles).



5. Conclusions

The origin of the NICMOS dark current anomaly remains unknown. Despite the fact that the test program could not produce new insight into the nature of the bump, it provides the most detailed dark current measurements of a NICMOS3 chip to date. The program thus constitutes a valuable resource for calibration programs of similar detectors.

The implications for NICMOS science operations during Cycle 10 and beyond also remain somewhat unclear. Assuming the trap hypothesis is correct, the dark current levels during NCS operations will depend to a large extent on the time constants for filling the traps and releasing the trapped charge. If these time constants are very short, it is possible that NICMOS will indeed show dark currents up to 2 e^-/s in the temperature regime pro-

vided for operations with the NCS. The impact on sensitivity for certain types of observations has been discussed in ISR NICMOS-99-001. Under worst case assumptions, NICMOS sensitivity will be degraded by 0.3 mags for imaging of faint sources in certain filters. Although it is far from clear that this degradation will indeed materialize, it might be prudent to make conservative recommendations for users planning to propose for Cycle 10.

6. Appendix A

Table 2. Ramp segments for warmup profile

T_{Start} [K]	T_{End} [K]	ΔT [K]	Δt [h]	Rate [K/h]	$T_{Elapsed}$ [days]
63.427	63.599	0.172	12.0	0.0143679	0.5
63.599	63.740	0.141	6.0	0.0234283	0.75
63.740	63.993	0.253	7.2	0.0351463	1.05
63.993	64.234	0.241	3.12	0.0773583	1.18
64.234	64.713	0.479	3.36	0.1425375	1.32
64.713	65.899	1.186	4.8	0.2471250	1.52
65.899	69.298	3.399	12.0	0.2832125	2.02
69.298	72.350	3.052	12.0	0.2543875	2.52
72.350	78.0	5.65	24.0	0.2354083	3.52
78.0	79.672	1.672	7.2	0.2321375	3.82
79.672	80.874	1.202	4.8	0.2505125	4.02
80.874	83.236	2.362	8.4	0.2811667	4.37
83.236	85.492	2.256	7.2	0.3133583	4.67
85.492	88.388	2.896	8.4	0.3447958	5.02
88.388	63.427	-24.961	6.0	-4.160167	5.27