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NICMOS Dark Current Anomaly: Models and Test Plans

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ABSTRACT

The NICMOS dark current anomaly (the "bump") was a transient enhancement of the detector dark current observed during the on-orbit warmup of the instrument after its cryogen depletion in January 1999. We summarize our current understanding of the mechanism which causes the effect, and summarize plans to test the most likely scenario.

1. Introduction

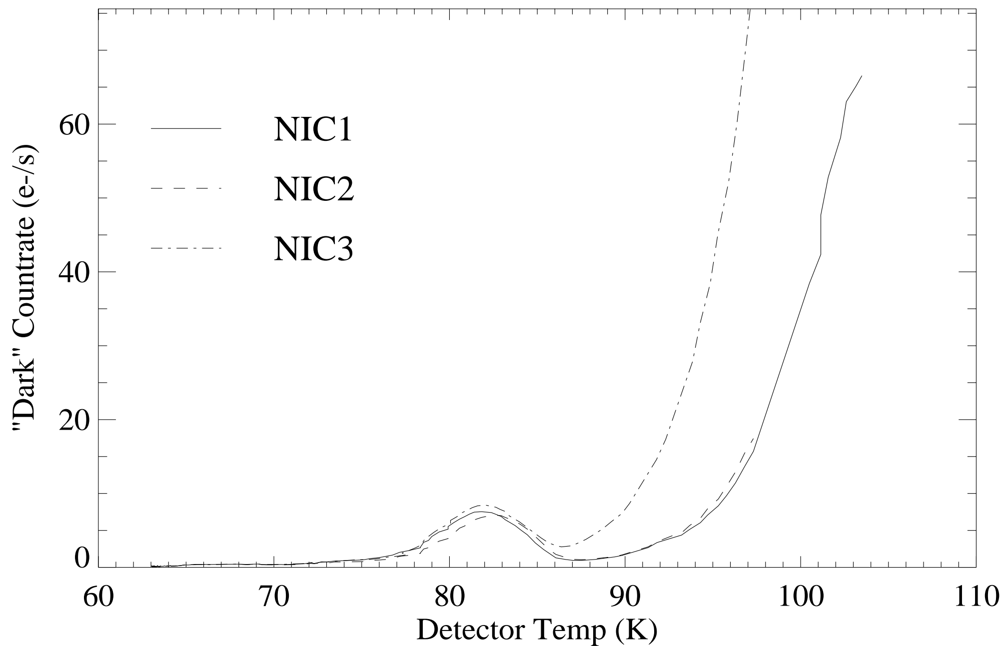
The NICMOS instrument suffered from a thermal short that caused the cryogen to evaporate at a higher than expected rate. The NICMOS lifetime thus was shortened to a little over two years, and the cryogen exhausted Jan. 4 1999. During the subsequent warmup of the instrument, detector parameters such as quantum efficiency and dark current have been extensively monitored, in view of the planned installation of the NICMOS cooling System (NCS). The NCS is a closed-loop cooler which will allow continuation of NICMOS operations, albeit at somewhat higher temperatures (~75 K compared to ~62 K during Cycle 7/7B). The results of the warmup monitoring program have been described in a previous ISR (NICMOS 99-001). One unexpected outcome was the behavior of the dark current as a function of temperature (Fig. 1). The increase and subsequent decline of the dark current between 78 K and 85 K (commonly referred to as the "bump") in all three NICMOS cameras is as of yet unexplained.

Because the bump is located at or close to the expected operating temperature for operations under the NCS, its nature needs to be understood for successful instrument calibration. In particular, it is important to answer the question whether or not the enhanced dark current will be observed during science operation in Cycle 10. The reason is that for long exposures, the NICMOS sensitivity is limited by the noise associated with the dark current signal. This was also recognized by the Independent Science Review panel chaired by M. Harwit. In its final report, the committee recommended "further labo-

ratory measurements of detector dark currents in order to provide a more secure estimate of this source of noise at detector temperatures that the NICMOS Cryocooler System (NCS) is likely to provide".

As a response to this charge, the NICMOS group at STScI has thus been seeking advice from detector manufacturers and theorists in order to identify possible explanations for the nature of the bump. We are pursuing a laboratory test program in collaboration with the NICMOS Investigation Definition Team (IDT) at the University of Arizona. The main goal of these tests is to confirm the general theory that electrons "trapped" in low-energy states within the detector material are responsible for the dark current bump. The idea is that at low temperatures, the electrons can not escape the traps, but as the detector material warmed up, the thermal excitation and subsequent release of the electrons caused a net increase in the dark current, until an equilibrium between capture and release rates was reached.

Figure 1: Median dark current signal vs. temperature for all three NICMOS cameras..



This ISR is organized as follows. We summarize in Section 2 the observational facts of the warmup monitoring program, and discuss how these can be used to rule out a number of explanations for the dark current bump. In Section 3, we give a description of those explanations that are consistent with the observations, and for each of those make some predictions that can be tested in the laboratory. We then discuss in Section 4 how the laboratory tests are set up, and to what degree they can discriminate between the competing scenarios.

2. Observational facts

i) Morphology of the dark current bump

One of the main results of the dark current monitoring program was that the spatial morphology of the signal caused by the bump closely resembled that of the detector quantum efficiency (DQE, Fig. 2). This fact was originally interpreted as evidence for a photonic origin of the bump, i.e. near-infrared (NIR) photons that are detected during the dark current exposures. These photons could be produced - for example - by some hot mechanical part inside the instrument. However, there are strong arguments against this notion (see next section). One conclusion one can draw from the DQE-like bump morphology is that the electrons responsible for the bump signal are subject to the same spatial variations in material properties as “normal” signal electrons. In other words, their detection probability is subject to quantities such as impurity density, mean free path length, or recombination efficiency. Therefore, the bump electrons are likely to originate at the same physical location as those electrons produced by detected photons during normal observations.

Also, an enhanced dark current due to a temporary rise in detector temperature can be ruled out because the signal morphology at dark current levels comparable to the bump (between 90 and 96 K, Fig. 1) is very different, and certainly does not reflect the DQE structure.

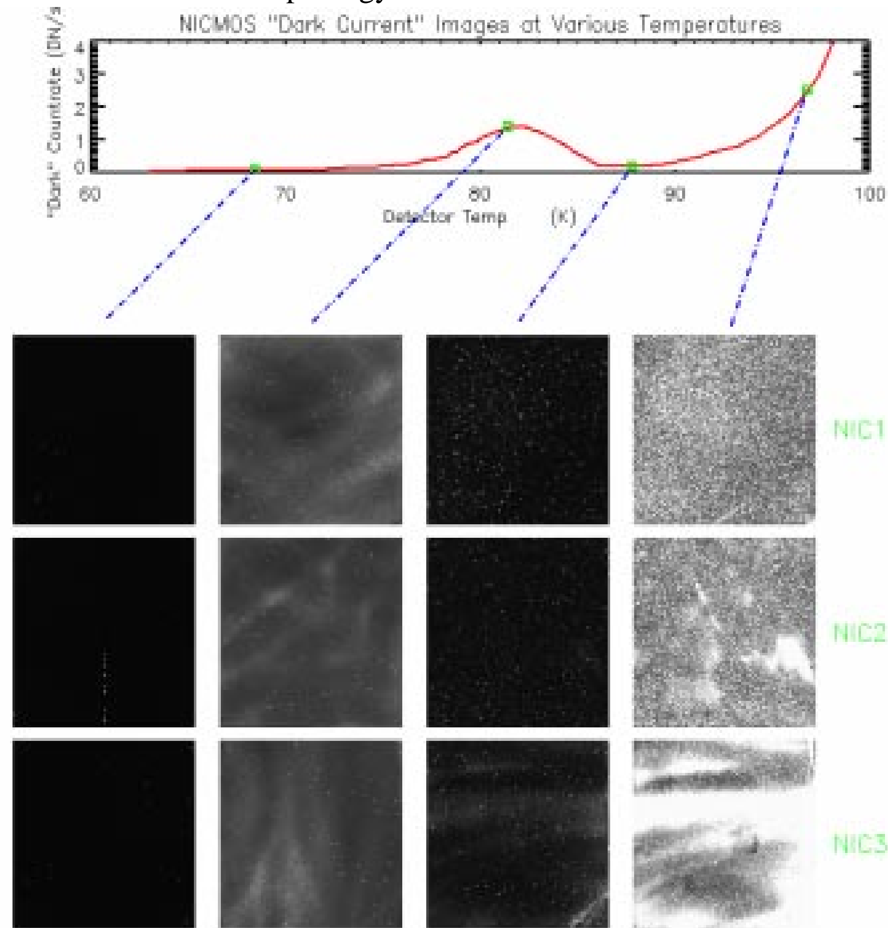
ii) Absence of the grot

Another important observational fact is that the dark current images taken over the duration of the bump do not show any signs for grot. Grot is the commonly used term for a number of small flecks of black paint on the detector surfaces. These particles presumably were scraped off the baffles during mechanical contact with the filter wheel housing, the process that led to the thermal short. Because grot prevents incoming photons from reaching the detector material, it is clearly visible in all NICMOS flat field images as clusters of “cold” pixels. The fact that the bump data do not show any grot clearly indicates that if NIR photons are indeed responsible for the bump, they must have come from within or behind the detector. No mechanism for producing NIR photons inside NICMOS is conceivable, because all temperature sensors showed a monotonic increase during the warmup. In addition, in order to produce such a close match to flat field exposures, the signal must have been produced in a pupil plane, which does not exist inside the filter wheel. One can therefore conclude that the bump signal can not be produced by NIR photons falling onto the detector.

iii) Conclusion

In summary, the only viable explanation for the origin of the bump at this stage is that a population of previously “trapped” electrons was released at temperatures between 78 and 85 K inside the detector material, and subsequently “swallowed” by the pn-junction, giving rise to the enhanced signal. Since these electrons were produced within the detector material, they naturally are subject to DQE variations. In what follows, we discuss in more detail possible models for the origin of such trapped electrons.

Figure 2: “Snapshot” dark exposures of all three cameras at temperatures of 68, 85, 98, and 116 K. Note the flatfield morphology in all cameras at 85 K



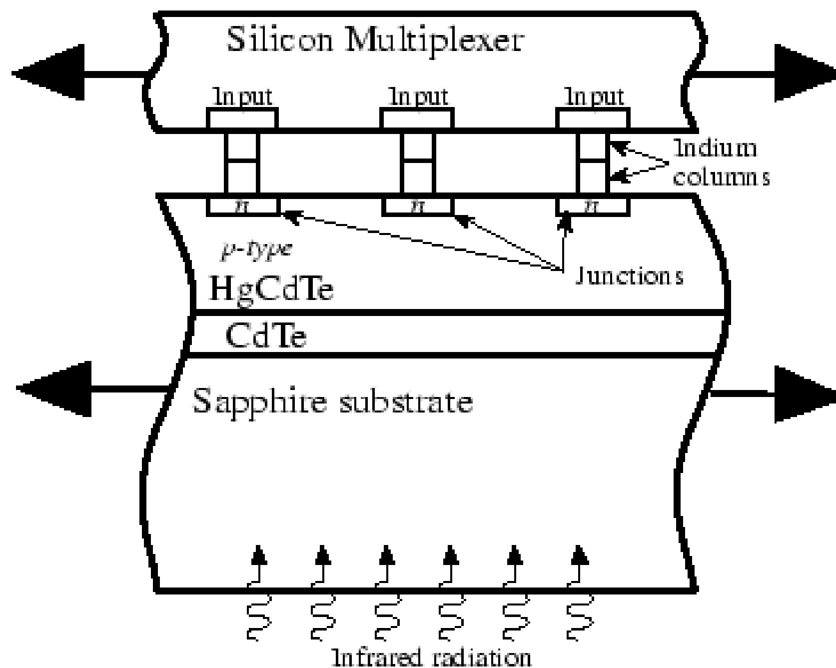
3. Models for the bump

In order to assess the impact of the dark current anomaly on the performance of NICMOS when operated with the NCS, the origin and physical nature of the traps that give rise to the bump must be understood. The STScI NICMOS Science Team has consulted extensively with the manufacturer of the NICMOS IR detectors, Rockwell, as well as with recognized experts in IR detector physics and operation. As a result of this investigation, it has been concluded that displacement damage due to exposure to high-energy protons in

the HST low-earth orbit (LEO) environment is unlikely to be the cause of the traps. The possibility that radiation damage could have caused the traps was discussed with experts at Rockwell. Based on radiation testing of the NICMOS arrays conducted by Rockwell, it has been concluded that the level of radiation exposure experienced by the flight arrays on-orbit is insufficient to produce the bump anomaly. For this reason, the focus of the investigation has shifted from traps caused by radiation damage to traps introduced into the detectors during manufacturing and processing.

Rockwell has proposed that a population of traps is located at or near the CdTe-HgCdTe interface in the photosensitive part of the hybrid FPA. The NICMOS detectors were fabricated using Rockwell PACE technology. In a PACE array, a buffer layer of CdTe is grown on a sapphire substrate. The photosensitive HgCdTe material is deposited on the CdTe buffer layer. Traps may have formed at the CdTe-HgCdTe interface, possibly because of the lattice mismatch between the two materials (Fig. 3). On average, ~5.8e5 e^-/pixel were detected over the temperature range of the bump.

Figure 3: Schematic of a PACE hybrid array. The suspected location of the charge traps is at the CdTe-HgCdTe interface.



Comparison of the spatial morphology of the dark current at the peak of the bump to that of the DQE has shown that the structure in the bump correlates most closely with the DQE at a wavelength of ~2 microns. According to Rockwell, a 2 micron photon incident on the backside of the detector (the sapphire substrate surface) will be absorbed in the vicinity of the CdTe-HgCdTe interface. Spatial variations in the carrier lifetime of the pho-

toelectrons give rise to the morphology observed in the 2 micron DQE. The spatial variation in the carrier lifetime of electrons liberated from traps at the CdTe-HgCdTe interface will be the same. The Rockwell hypothesis is therefore qualitatively consistent with observation in that it predicts correlation between the morphology of the dark current bump and the 2 micron DQE.

Empirical verification of the Rockwell hypothesis requires that some means be devised to determine where the traps are located in the bulk of the detector. The 2 micron DQE correlation cannot be considered definitive because it is based on comparing broadband flats to the dark current images at the peak of the bump. A study of the correlation between the morphology of the bump and the spatial structure of flats taken through a series of narrowband filters may lead to a better understanding of where the traps are located relative to the CdTe-HgCdTe interface.

An alternative hypothesis has been advanced by Mr. Thomas Casselman of C-Fourth Consultants. In contrast to the Rockwell hypothesis, he proposes that the traps are due to surface states located at the front interface of the HgCdTe material. Epoxy is injected between the silicon multiplexer and the HgCdTe halves of the hybrid sandwich to seal and strengthen the bump bond interface. The pn-junctions on the HgCdTe side of the bump bond interface are passivated with ZnS (Fig. 3). Passivation is used in both visible and IR detectors as an intermediate buffer layer between dissimilar materials, and/or to prevent surface currents between pixels. Casselman suggests that surface states may have formed at the ZnS/HgCdTe interface. In principle, the observed morphology in the dark current bump can be explained by the this hypothesis as being due to spatial variations in the density of the surface traps. It is less clear, however, how the surface states at the passivation interface can cause correlated structure in the 2 micron DQE.

The currently favored explanation for the NICMOS dark current anomaly can then be summarized as follows. Initially, i.e. immediately after the cooldown, the traps would be empty. As soon as free electrons are generated by IR photons during illumination of the detector, the traps can capture electrons. After capture, the electrons stay inside the trap as long as the detector is kept cold, because during normal operations, there is no excitation mechanism to free them again. However, during warmup, the detector material reaches a temperature threshold above which thermal excitation can cause the release and subsequent detection of the trapped electrons . The test program described in the next section is designed to check the predictions of this scenario.

4. General Test plan

The history of the NICMOS flight detectors is unique in the sense that they were kept continuously cold for about four years. During this time span, which included the pre-launch test program and the on-orbit lifetime, they were extensively illuminated, both through calibration (flat-field) and science exposures. To our knowledge, laboratory dark

current measurements for infrared devices have not previously been performed under similar conditions, i.e. after the detector has been illuminated in the cold state. It is therefore entirely possible that the NICMOS dark current bump is not an anomaly, but rather a natural consequence of the manufacturing process which should be reproducible.

Our current test plan therefore has the primary goal of confirming the viability of the proposed mechanism for the dark current bump via trapped electrons that are released at a certain temperature threshold. The idea is to reproduce the on-orbit history of the NICMOS detectors as closely as possible in the laboratory, under the constraints of a time- and cost-limited program.

The NICMOS Investigation Definition Team at the University of Arizona is in possession of a number of NICMOS flight spare detectors, some of which are from the same manufacturing lot as the on-orbit detectors. We will use one of these devices for our test sequence:

1. Cool down of the detector to about 60 K in a dark environment.
2. Monitor dark current during a controlled warmup to about 90 K. The temperature profile for the warmup will be a close approximation to the actual on-orbit profile of the NICMOS warm-up after cryogen exhaustion. This sequence is intended to serve as a baseline measurement of the detector dark current. It is "traditional" in the sense that the detector is not illuminated prior to the dark current measurements.
3. Cool down back to 60 K with the detector still in a dark environment.
4. Illuminate the detector to an accumulated level similar to that seen by the flight detectors over both the pre-launch tests and the on-orbit lifetime. Quantitative measurements of the actual illumination levels will be obtained by reading out the device. It is desirable, but not critical, that the illumination is uniform across the chip.
5. Repeat step 2).

If the comparison of the measured dark current with the "baseline" levels obtained during step 2) reveals enhanced dark current in the range 78-85 K, the proposed scenario can be considered as confirmed. The structure of the dark current should be compared to the spatial DQE variations of the chip. If these are not known from previous use of the chip, flatfield measurement are needed, either during this test or later. A positive detection of the bump phenomenon might warrant further tests to constrain better the nature of the charge traps, i.e. to determine their energy levels, physical location, and the time constants governing the capture and release of electrons.

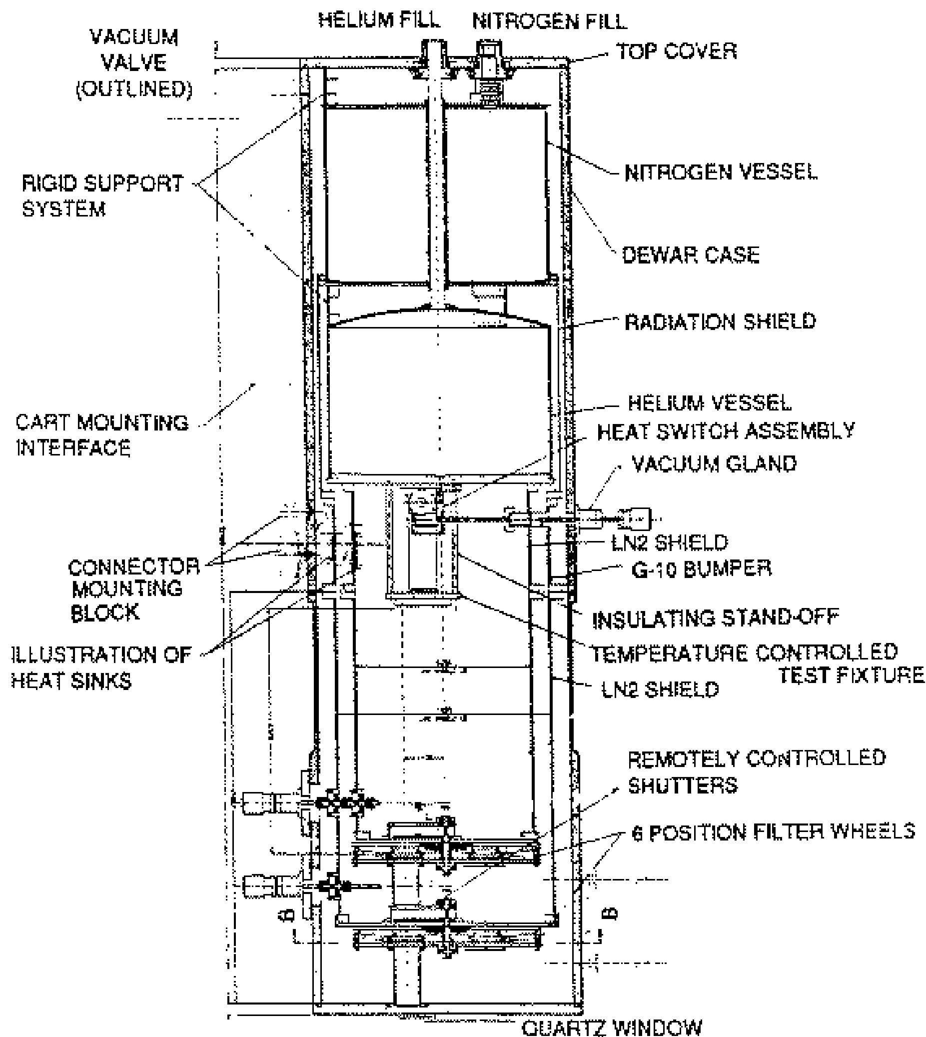
An additional test is intended to verify that the warm-up speed of the detectors after the cryogen exhaustion does not give rise to non-equilibrium effects. It is known that NICMOS arrays show unpredictable behavior when not in thermal equilibrium, and enhanced

dark current is quite possibly a consequence of a sudden temperature transitions of the detector. In this case, however, it is somewhat difficult to understand why the enhanced dark current should trace the DQE. To rule out this scenario, we will repeat steps 1 and 2, but instead of a continuous temperature rise with a gradient of about 7 K/day, we will let the detector equilibrate at a number of temperatures before measuring the dark current.

5. Laboratory Equipment and Performance

The test setup at UofA comprises a liquid helium dewar (Fig. 4) with a cold detector stage. A heater system controls the detector temperatures to predefined setpoints. A large number of linear ramps are programmable, so that the NICMOS warm-up profile can be closely approximated.

Figure 4: Schematic of the dewar system used for the tests at UofA



The dewar has a cold shutter to ensure dark conditions. Preliminary tests have demonstrated that the dewar is indeed dark to levels around 0.3 e^-/s. For comparison, the average "bump-free" on-orbit dark current within the NICMOS instrument was about 0.1 e^-/s, with the bump being at levels of 2-3 e^-/s. The system should therefore be well suited for the purpose of these tests. For the illumination of the detector, the shutter can be opened, and light can enter through the dewar window. Since the window is located at the bottom of the dewar, we plan to use the thermal emission from the warm laboratory floor as a light source.

The readout electronics is based on a CCD controller manufactured by InfraredLabs and modified for infrared use. In order to avoid the need for excessively long integration times, the read noise of the system should be as low as possible. As an example, assume a typical dark current level of 0.3 e^-/s for the non-bump regime. In order to detect such a signal at the 5 σ level after 1000 s of integration, the read noise needs to be lower than 60 e^- RMS. A read noise twice as high, i.e. 120 e^-, would require 2000 s of integration time, which we consider the maximum useful integration time, given typical warmup rates around 0.3 K/hr. For comparison, the typical on-orbit readout noise during the NICMOS lifetime was 35 e^- per readout pair.

The electronics is set up to use the standard MULTIACCUM STEP 64 sequence that was used in the warm-up monitoring program, and we will read out the detector during the test with the same sequences as used on orbit. The data will be transferred in FITS format to a Sun workstation where they can be analyzed in an almost real-time fashion. The STScI NICMOS group will send personnel to Tucson for the duration of the test to allow a rapid analysis of the data. Results of the test program are expected before the end of the year, and will be summarized in another ISR.

6. Summary

The described program is intended to offer a cost-effective way of testing a viable explanation for the NICMOS dark current anomaly and to decide whether science observations in Cycle 10 will be affected by the enhanced dark current. In case the currently favored explanation of a sudden release of previously trapped electrons proves to be consistent with the test results, one can be reasonably confident that NICMOS performance will be the same as during Cycle 7/7A. More detailed tests might then be desirable to further constrain the processes that produce such a population of charge traps. Ultimately, this might lead to improved manufacturing processes for solid state devices.